CONVERSION OF THE D37C COMPUTER FOR GENERAL PURPOSE APPLICATIONS

THESIS

GE/EE/74-16

Dennis C. Reguli
2Lt. USAF

Approved for public release, distribution unlimited.

Unclassified

SECURITY CLASSIFICATION OF THIS PAGE (When Date Entered)

REPORT DOCUMENTATION PAGE		READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER GE/EE/74-16	2. GOVT ACCESSION NO.	3. RECIPIENT'S CATALOG NUMBER
4. TITLE (and Subtitle) CONVERSION OF THE D37C COMPUTER FOR GENERAL PURPOSE APPLICATIONS		5. TYPE OF REPORT & PERIOD COVERED MS Thesis 6. PERFORMING ORG. REPORT NUMBER
7. AUTHOR(s) Dennis C. Reguli 2Lt. USAF		8. CONTRACT OR GRANT NUMBER(s)
9. PERFORMING ORGANIZATION NAME AND ADDRESS Air Force Institute of Technology (AFIT-EN) Wright-Patterson AFB, Ohio 45433		10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS
11. CONTROLLING OFFICE NAME AND ADDRESS		12. REPORT DATE March, 1974 13. NUMBER OF PAGES 168
14. MONITORING AGENCY NAME & ADDRESS(if different from Controlling Office)		15. SECURITY CLASS. (of this report) 15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18. SUPPLEMENTARY NOTES

Approved for public release; IAW AFR 190-17

Capt. Jerry Hix USAF

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Minuteman II Computer

D37C Computer

Minicomputer, general purpose

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This report addresses the problem of reutilizing later Minuteman computers, D37C's, which will become surplus in the near future. Revitilization is assumed optimum by first converting into a general purpose minicomputer. This is done for the D37C by supplying external support systems, control and monitor circuits, and expanded I/O capability. The external systems include power supplies and cooling system and were provided at AFIT by laboratory generators and a fan and pump assembly, respectively. The

DD FORM 1 JAN 73 1473 EDITION OF 1 NOV 65 IS OBSOLETE

Unclassified

SECURITY CLASSIFICATION OF THIS PAGE (When Date Entered)

generators produce the 28vdc at 15 amp and the 22vrms, 400 Hz, 3Ø current required by the computer and the cooling system provides less than continuous duty cycle cooling. The Control and Monitor circuits are required to control the mode transitions of the machine and to monitor the results. The simple circuits required were expanded to include a program load scheme using a multiplexed output, Mpx. The final Control and Monitor system will provide sufficient I/O capabilities for many applications, however, an expanded I/O system was developed for more versatility. The expanded I/O system provides for program controlled I/O, a parallel data bus for an I/O port, and a speed increase of 50 words per second to 100 plus.

CONVERSION OF THE D37C COMPUTER FOR GENERAL PURPOSE APPLICATIONS

THESIS

GE/EE/74-16 Dennis C. Reguli
2Lt. USAF

Approved for public release, distribution unlimited.

CONVERSION OF THE D37C COMPUTER FOR GENERAL PURPOSE APPLICATIONS

THESIS

Presented to the Faculty of the School of Engineering
of the Air Force Institute of Technology

Air University

in Partial Fulfillment of the
Requirements for the Degree of

Master of Science

by

Dennis C. Reguli, B.S.E.E.
2Lt. USAF

Graduate Electrical Engineering

March 1974

Preface

In this report I have tried to show that a Minuteman guidance and control computer, the D37C, can be converted for general purpose applications through the addition of a few simple circuits and systems. I hope my efforts will assist the Air Force in reutilizing these machines in laboratories or at least, I expect my work to be the foundation for further study in reutilizing these machines by civilian institutions.

This investigation considers only hardware systems added to the machine and does not include software development or machine modifications. In short, any graduate or advanced undergraduate student in Electrical Engineering may use my work and a bare D37C computer to produce a versatile, general purpose minicomputer. The essential elements for this conversion are included in the circuit descriptions and schematics of Appendices B and C.

I wish to acknowledge my indebtedness to several individuals in the preparation of this report. I thank Messrs. Wells, Fisher, and Kuchenbecker for their technical assistance through telephone interview. Thanks also goes to Prof. Lamont, my thesis advisor, for his motivational force and patience with broken deadlines. Messrs. Wolfe, Short, and Bayard were of great assistance in constructing some portions of the console. I am deeply indepted to lab partners Lt.'s Lundy and Kennedy whose casual conversations helped solve many problems. Final-

ly, I wish to express sincere thanks to my wife who helped in proof reading and persisted through weekends and evenings of neglect.

Dennis C. Reguli

Contents

Contents

Contents

List of Figures

List of Tables

Abstract

Since the Air Force surplused Minuteman guidance computers there has been an interest in reutilization by civilian institutions. This report addresses the problem of reutilizing later Minuteman computers, D37C's, which will become surplus in the near future. Revitilization is assumed optimum by first converting into a general purpose minicomputer. This is done for the D37C by supplying external support systems, control and monitor circuits, and expanded I/O capability. The external systems include power supplies and cooling system and were provided at AFIT by laboratory generators and a fan and pump assembly, respectively. The generators produce the 28vdc at 15 amp and the 22vrms, 400 Hz, 3ø current required by the computer and the cooling system provides less than continuous duty cycle cooling. The Control and Monitor circuits are required to control the mode transitions of the machine and to monitor the results. The simple circuits required were expanded to include a program load scheme using the character inputs, and a register display output using a multiplexed output, Mpx. The final Control and Monitor system will provide sufficient I/O capabilities for many applications, however, an expanded I/O system was developed for more versatility. The expanded I/O system provides for program controlled I/O, a parallel data bus for an I/O port, and a speed increase of 50 words per second to 100 plus. The converted D37C final system will provide many institutions with a highly reliable and versatile minicomputer.

I. Introduction

This is a report on developing a process to convert the Minuteman guidance and control computer, the D37C, into a general purpose minicomputer. The introduction will discuss previous work in the general area, state explicitly the problems of development, describe the basic machine structure, and provide some insight into the scope and organization of the remaining report. This report assumes the reader has some Electrical Engineering background and comprehends basic digital logic circuits and Boolean Algebra. It would also be helpful, though not necessary, for the reader to be familiar with basic computer input/output (I/O) operations.

Background

This familiarization section begins with the history of surplus Minuteman computers, the formation of the Minuteman Computers Users Group and an overview of work in this area at the Air Force Institute of Technology. A short section on references follows to explain the sources for this report.

History. In the early 1960's the United States Air Force surplused over 400 Minuteman guidance and control computers, the D17B, through a modernization program. These ICBM computers were released to government activities, industrial contractors, universities and other organizations for the purpose of research, education, and other applications (Ref 6). These machines, costing originally about $234,000 each, are supplying these organizations with low cost computing power. A

measured mean-time-between-failures of 5.5 years and environmental design criteria make the D17B a highly reliable and rugged device (Ref 6).

The new owners of these machines, desiring to use the D17B to its fullest capacity, formed an organization for effective information transfer. This group is called the Minuteman Computer Users Group (MCUG) and is headed by Dr. Charles H. Beck of Tulane University, New Orleans, Louisiana. To date, the group has made significant advances in hardware modifications, software routines, and special applications development for the D17B. They have developed a hardware divide for the machine, programs for simulating the D17B, an assembler, hybrid and analysis systems, and more (Ref 6). One machine has been shown cost effective for blood serum analysis at the Walter Reed Army Institute of Research, Walter Reed Army Medical Center (Ref 6).

The Air Force Institute of Technology (AFIT), which has two D17B's, is an active member of MCUG, and is deeply involved in revitalizing these machines. Using the machines primarily as educational tools, AFIT's students are investigating conversion of the D17B for general purpose use. In a general purpose configuration the machines could easily suit a wide range of applications, therby aiding their use by MCUG and AFIT. If the conversion is sufficiently sound the Air Force could recover some of their cost by reutilizing them in their own laboratories. Toward this end, AFIT students have written seven Masters Thesis on making the D17B more versatile and suitable

for general use. This work has included console development (Ref 8), peripheral device interfacing (Ref 14), and expansion of Input/Output capabilities (Ref 15).

In the spring of 1972 AFIT received a new addition to their Minuteman computer laboratory, the D37C, on loan from the Air Force Logistic Command. This newer model of the D17B is expected to be surplused in the same manner. Because of technological advances the D37C is physically smaller, has more instructions, and almost twice the memory of the older machine. AFIT received an operational D37C early because, for some defect, it is non-flight worthy. This machine is to be investigated for the same prospect of general purpose conversion. This is the first thesis concerned with converting the D37C computer for general purpose applications.

References. The needed information for this report was found in Air Force documents on the D37C prepared by Autonetics, thesis' of AFIT students written on AFIT's Minuteman system, and direct conversation with engineers involved with the machine. The documents include Repair and Recycle Specifications, Programming Manual, System Depot Overhaul, Logical Description, and Logic Breakdown manuals for the D37C computer. Because of the similarities in the D17B and D37C, AFIT students' thesis on the D17B have proven very helpful in designing the displays and I/O expansion. For specific information not available in the aforementioned documents, direct conversations with Messrs. Wells, Fisher, and Kuchenbecker were invaluable. Mr. Wells is an engineer at the Minuteman

Test and Repair Center, Newark Air Force Station, Newark, Ohio. Messrs. Fisher and Kuchenbecker are engineers at the Autonetic's plant where the computer was built in Anaheim, California. All of the Air Force documents, AFIT thesis, and other references used for this report are listed in the bibliography.

The documents at AFIT available for the D37C are not as complete as those for the D17B. There are only a few general schematics, but every signal available at the interface plugs is well defined. This lack of documentation is not a handicap for this report or others not involving hardware modifications of the machine. However, for work in this area one might contact the aforementioned gentlemen for information concerning complete schematics.

Problem Statement

This section will state the D37C conversion problems considered in this report. It will then mention the constraints involved and the method of attack chosen.

Problems. In general, converting the D37C computer for general purpose use involves supplying external support systems, building monitor and control circuits, and expanding its I/O capabilities. These problems are listed and expanded below:

1) External Support Systems - The support systems include two power supplies required for computer operation that are not in the computer housing. It also includes a cooling system sufficient to maintain the environment required

by the circuitry.

2) Control and Monitor Circuits - The control and monitor circuits shall provide an easy method of controlling the computer's modes and provide for a simple memory loading scheme. It shall also provide a means for monitoring the the computer's major modes and checking the contents of selected registers.

3) I/O Expansion - The input/output capabilities of the machine should be expanded to include a programmed controlled I/O scheme enabling the computer to communicate with standard minicomputer peripherals such as tape punch, tape reader, teletype, and others. It should also be compatible with existing Minuteman systems at AFIT.

Constraints. When searching for solutions to these problems certain constraints must be considered. The main constraint is the basic capabilities of the computer. Since it was designed for a special application it has a special instruction set, special I/O signals, and is inherently slow (clock rate is approximately 350KHz). Because of these restrictions it cannot be converted to perform in the category of HP-2100's or PDP-12's which were designed as general purpose minicomputers. The process of converting the D37C into a general purpose computer should be simple and inexpensive while still producing a machine that is easy to use and useful in general applications. A simple conversion process would be easy to construct, troubleshoot, maintain, and provide an uncomplicated foundation for further study. An inexpensive process would

aid the revitalization of these machines by civilian organizations. Equipment required for conversion is restricted by availability. Because of the time required to receive new or special equipment, the parts used in this report are those that were either on hand or easily obtainable. It is also desired that all systems be versatile, non-restrictive to future work, and compatible with present AFIT Minuteman systems.

Method of Attack. The method of attack is a step by step, feedback process to choose the best solutions to the stated problems. Since there is little overlapping of the problems, each one is considered separately while keeping in mind the complete and final system. After the criteria for solving a problem is set, all reasonable solutions are considered. After selecting a solution based on the above mentioned constraints, it is designed and implemented. Once built, it is tested against the original criteria. A selected solution must cover the requirements specified in the problem statement and fall within the boundries of the constraints to be accepted. If it fails this test or a better method is discovered, it is discarded and an alternate solution is designed, built, and tested.

Basic D37C Computer Description

This section describes the basic characteristics of the D37C computer, first by comparing it to the D17B then by discussing the memory, processor, and I/O units in more detail. This is intended only as an introduction to the machine. For a more detailed description see Appendix A.

D17B Comparison. Both the D17B and the D37C computers were designed and built by Autonetics, a division of North American Rockwell, for the real time purpose of guiding and controlling an ICBM from launch to detonation. Because of this, there are many basic similarities between the two. They are both synchronous, serial machines with fixed head disks for primary memory. They have two-address instructions, half and whole word precision, and many similar instruction operator codes. The differences in the two computers are based mainly upon their differing technologies. The D17B was built in 1962 using transistors and other discrete components to realize its logic circuits (Ref 6). On the other hand, the D37C was built in 1964 using small scale integrated circuits and discrete components only in the internal power supplies. Table I Summarizes the comparison of the two Minuteman computers.

D37C Characteristics. The D37C computer consists of four main sections; the memory, the central processing unit (CPU), and the input and output units. These sections are enclosed in one case shown in Fig. 1.

The memory is a two-sided, fixed head disk which rotates at 6000rpm. It contains 7222 words of 27 bits. Each word contains 24 data bits and three spacer bits not available to the programmer (Ref 4). The memory is arranged in 56 channels of 128 words each plus ten rapid access channels of one to sixteen words. The memory also includes the accumulators and instruction register (Ref 3).

Table I.

Comparison of D17B and D37C

Model	D17B	D37C
Year	1962	1964
Type	Serial, Synchronous	Same
Number System	Binary, fixed point, 2's complement	"
Data Word Length	11 or 24 bit (double-precision)	"
Instruction Word Length	24 bit	"
Number of Instructions	39	57
Execution Times:		
Add	78 1/8 us	Same
Multiply	1 ms	"
Divide	(software)	2 ms
Clock Channel	345.6 KHz	Same
Addressing	Direct of entire memory	Direct w/in Bank ($\frac{1}{4}$ of memory)
Memory:		
Word Length:	24 bits plus 3 timing	Same
Type:	Ferrous oxide-coated NDRO disc	"
Cycle Time:	78 1/8 us minimal	"
Capacity:	5,454 or 2,727 words (double precision)	14,444 or 7,222 words
Input/Output:		
Input Lines:	48 digital	65 digital 32 analog
Output Lines:	28 digital 12 analog 3 pulse	45 digital 16 analog 8 pulse
Program:	800 5-bit characters/sec	Same
Physical Characteristics:		
Dimensions:	20" high, 29" diameter	20.9 x 6.9 x 9.5 inches
Power:	28vdc$\pm$1v at 19A	28vdc$\pm$1.7v at 15A
Circuits:	Discrete DRL and DTL	IC DRL and DTL
Software:	Minimal delay coding machine language modular special-purpose subwriting	Same
Reliability:	5.5 years MTBF	(classified)

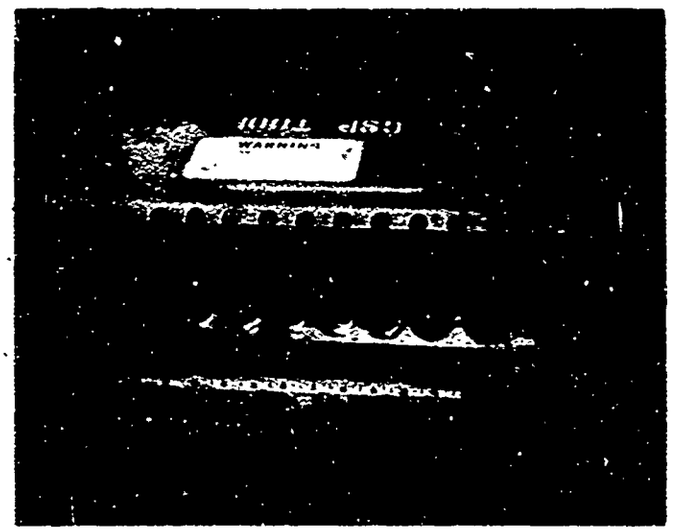


Figure 1. Photograph of a D37C Computer.

The central processor (CPU) is a serial device realized from small scale integrated circuits using diode-transistor logic. It contains 57 instructions including hardware multiply and divide. They also include provisions (flags) for altering or repeating instructions. The CPU operates on data in the full word (24 bit) or half word (11 bit) mode. Data is represented as binary fractions in sign plus two's complement representation (Ref 3).

Both Minuteman computers contain elaborate input/output units. These units are designed for real time operations of gyro sensing and torquing, accelerometer reading, gimbaling rocket engines and arming nuclear warheads. Because of the specialized nature of these I/O units they are not directly compatible with usual minicomputer peripherals. Overcoming this difficulty and adapting the I/O units to a more conventional I/O scheme is the topic of a thesis by Lt. Joseph Theriault entitled Design Expansion of the D17B Computer Input/Output Facility for General-Purpose Applications. Adapting the D37C's I/O units is the topic of Chapter IV. The input/output signals, as well as the memory and CPU, are defined further in Appendix A.

Scope and Organization

This section defines the scope of this report, explains some of the conventions used, and describes the structure of the remaining text.

Scope. This paper provides the foundation for future work on converting the D37C computer for general use. It does

so by providing solutions to the problems involved in initial set-up and operation of the D37C. This report also presents alternate (some untried) solutions in case the ones chosen here are impractical in other situations. There is enough information in the body and appendix to allow an average Electrical Engineering graduate student to perform equivalent work on a bare D37C computer.

Conventions. In order to maintain some consistency with Minuteman documents and previous thesis, and to minimize confusion, certain conventions will be maintained throughout this report. Complemented literals in logic expressions are represented with an appostrophe rather than an overline, i.e. A' = $\overline{A}$. Positive logic will be used throughout except where indicated. Signals are renamed after they are interfaced (level shifted). The new names are acronyms which better represents the signals' purpose or they have one or two letters missing from the original label. Naming intermediate signals in a circuit has been kept to a minimum to avoid confusion.

Wiring labels for circuits are given in three alphanumeric numbers as shown and explained below:

I1-32-3
1) 2) 3)

1) I1 - indicates the board. This term will always start with a letter and may be omitted if the entire schematic is on the same circuit board and diagram.

2) 32 - indicates an IC socket or socket location. This number can range from 1 - 35 and may be omitted if the intended socket is the card end connector.

3) 3 - indicates a pin location. This can range from 1 - 24.

Structure. A structure was selected to present the material in the most logical and least confusing manner. Each problem investigated is presented in a separate chapter because the problems are relatively independent. As a result, each chapter is relatively independent, containing all necessary information for that section and leaving unnecessary details for the appendix. Each chapter will contain the specifications, organization, design, and implementation for that section of the system. This structure aids the report's utilization as a handbook for building an equivalent system or as a guide for troubleshooting and maintenance. Because of the separateness of the chapters, they may be removed, updated, or added to with relative ease.

II. External Support Systems

This chapter describes and develops the external power supplies and cooling system necessary for operating the D37C computer. The power supplies and cooling system are presented separately because the two are relatively independent systems as shown by the functional block diagram.

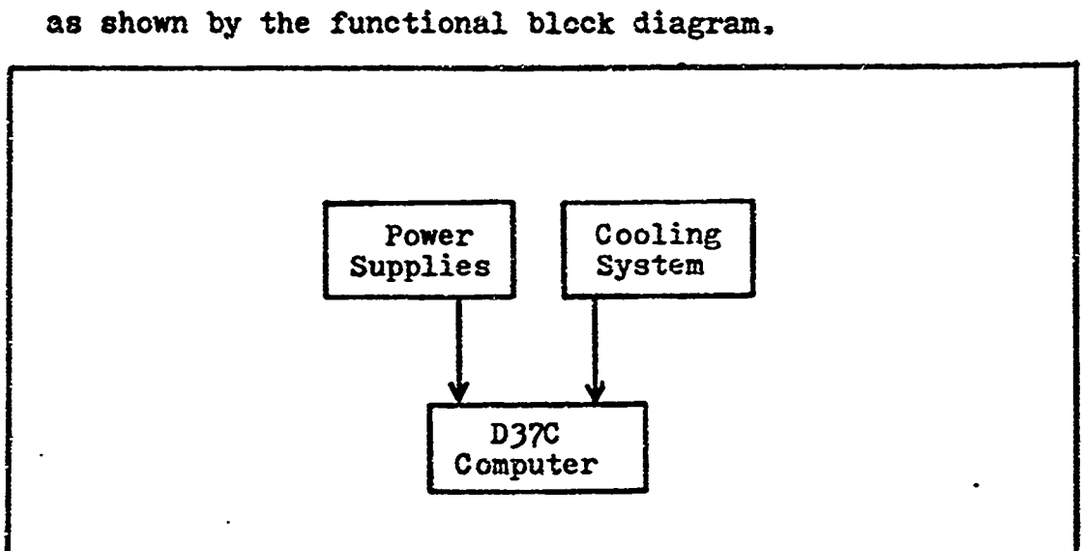


Figure 2. External Support Systems, Block Diagram.

Power Supplies

Specifications. There are two external power supplies required to operate the D37C computer. One is a 28v DC supply required for the electronics and the other is a 400Hz AC supply for the memory motor (disk memory). Specifications for the electronic's power supply require +28.0±1.70 volts at 15 amperes maximum. Ripple and noise is restricted to 60 millivolts peak to peak maximum and the supply's internal impedance shall be as follows (Ref 5):

Frequency	Impedance (ohms)
dc to 1 KHz	< .05
1KHz to 100KHz	< 0.7
100KHz to 500KHz	< 6

The memory motor supply shall be 3-phase, 3-wire AC with a frequency of 400±4Hz. Phase rotation shall be ABC with displacement between adjacent phases of 120±2 degrees. Steady-state peak voltage between phases shall be 27.25±0.82 volts. Current required is 4.5 amperes per phase with peaks of 10 amperes for no more than 4 seconds (Ref 5). The AC wave form specified is in Fig. 3.

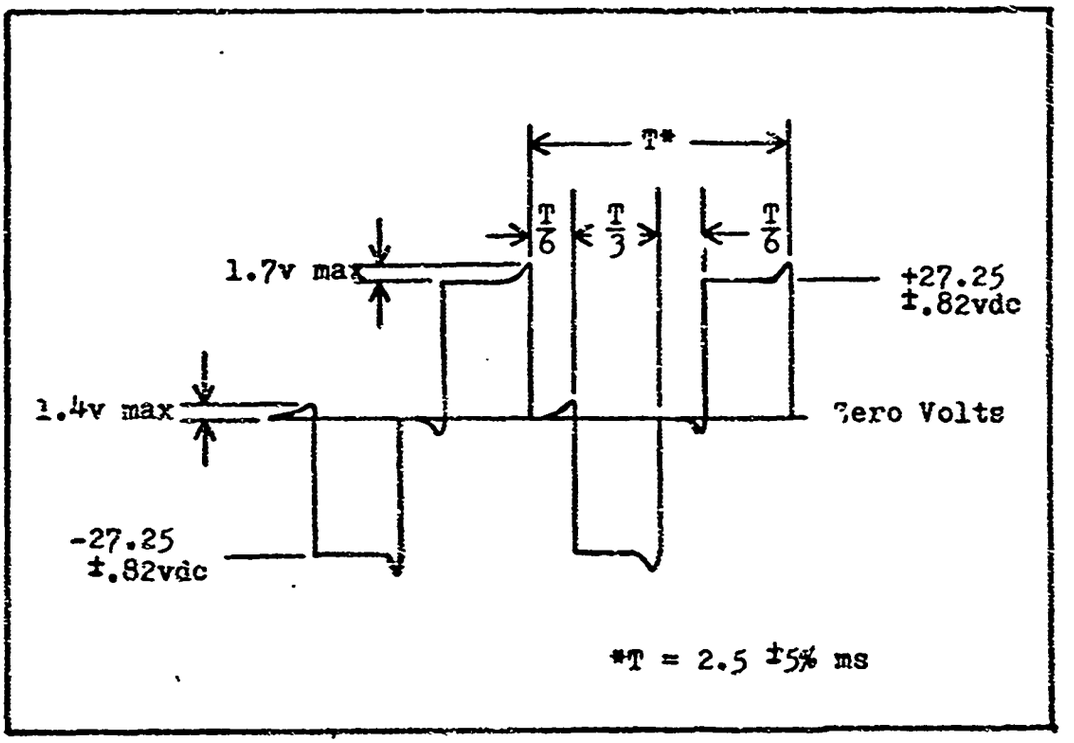


Figure 3. Specified Memory Power Wave Form.

There are a few additional requirements concerning the computer's external power supplies. For instance, primary

power (28vdc) must be disabled within 10 milliseconds if the voltage exceeds +30.3vdc. Also, modules should not be installed or removed from the computer chassis if any power is on except memory power. Memory power may be on with primary power off but the converse is not true. Also primary power should not be on without a complete set of modules in the machine. At initial turn on only, over-current surges may exist for a maximum of 45 milliseconds. Finally, the memory power current should stabilize at 3.3 ampere or less when the disk reaches synchronous speed (or approximately six seconds after turn on) (Ref 5).

Organization. The specifications mentioned are those required for a test situation in which the conditions on board the rocket must be simulated. The primary power specifications, therefore, are designed to simulate a battery or battery-generator source in the missile. It is also assumed the memory power requirements are designed to simulate the output of a solid state AC generator package which is also on board the missile. Because of the criteria behind the strict power specifications, it may be necessary to relax the requirements in order to utilize available equipment. For instance, conversations with Mr. Fisher and examination of surplus memory test equipment indicate the memory waveform may be replaced by a 22vrms sine wave. This is important because in many applications a 400Hz sine wave will be much easier to produce than the specified waveform.

Many solutions to the external power problem become pos-

sible if one keeps in mind that specifications may be relaxed for a less harsh environment such as a classroom or laboratory. Both supplies may be built from scrath or bought if commercially available. The primary power may be sourced from batteries, a power supply to convert line AC to 28Vdc, or by a motor-generator device. The memory power may be supplied by a circuit built to produce the specified waveform or by a motor-alternator combination to produce sine waves. There is also the possibility of converting a memory motor supply from a scrap D17B computer since the power requirements are very similar.

Design. The easiest available method of supplying power to the computer was chosen for AFIT's applications. This consists of taking advantage of an elaborate power generation and distribution system located in AFIT's school of engineering. A centrally located generator room is capable of supplying both the 28vdc at 15 amperes and the 400Hz 3 phase power for the memory motor. Power from this room is routed throughout the building and available at power panels in each laboratory. This system of power has proven sufficient and reliable for running a D17B computer which also requires 28vdc.

The power supply section of the computer console at AFIT includes step down transformers for the memory power and additional power supplies for console electronics. The normal operating range for AFIT's 400Hz alternator is 125 to 250V and is therefore unstable at 22vrms. To counteract this, transformers are used in the console to step down the voltage. The

computer power system is combined with power supplies for other circuitry to provide a centralized power location in the console. These additional supplies include regulated +5, +12, and -12vdc sources.

Realization. Implementing this type of power system involves fabricating cables to run the power from panel to console, building a distribution system inside the console, wiring step down transformers for memory power, and providing appropriate safeguards and power control. Fig. 4A shows a schematic of the computer power system. The dc power is provided with a 20 amp circuit breaker to control the power and to protect the computer from over currents. There are also circuit breakers on the power distribution panel for additional protection.

The memory power voltage is stepped down with two transformers. Each transformer is actually composed of two 6.3v filament transformers with the primaries in parallel and secondaries in series. The transformers were designed for 60Hz but operate well at 400Hz since the cores have less time to saturate. Each secondary can supply 6A continuously. The 22 vrms, 400Hz power is supplied to the computer when 180vrms is applied to the primaries. Switching memory power is done with the circuit breaker switch on the power panel.

The schematic for the console power supplies is shown in Fig. 4B. Power supplies salvaged from surplus equipment supply the regulated current required by the console electronics. Each is fused for its maximum output and switched with a com-

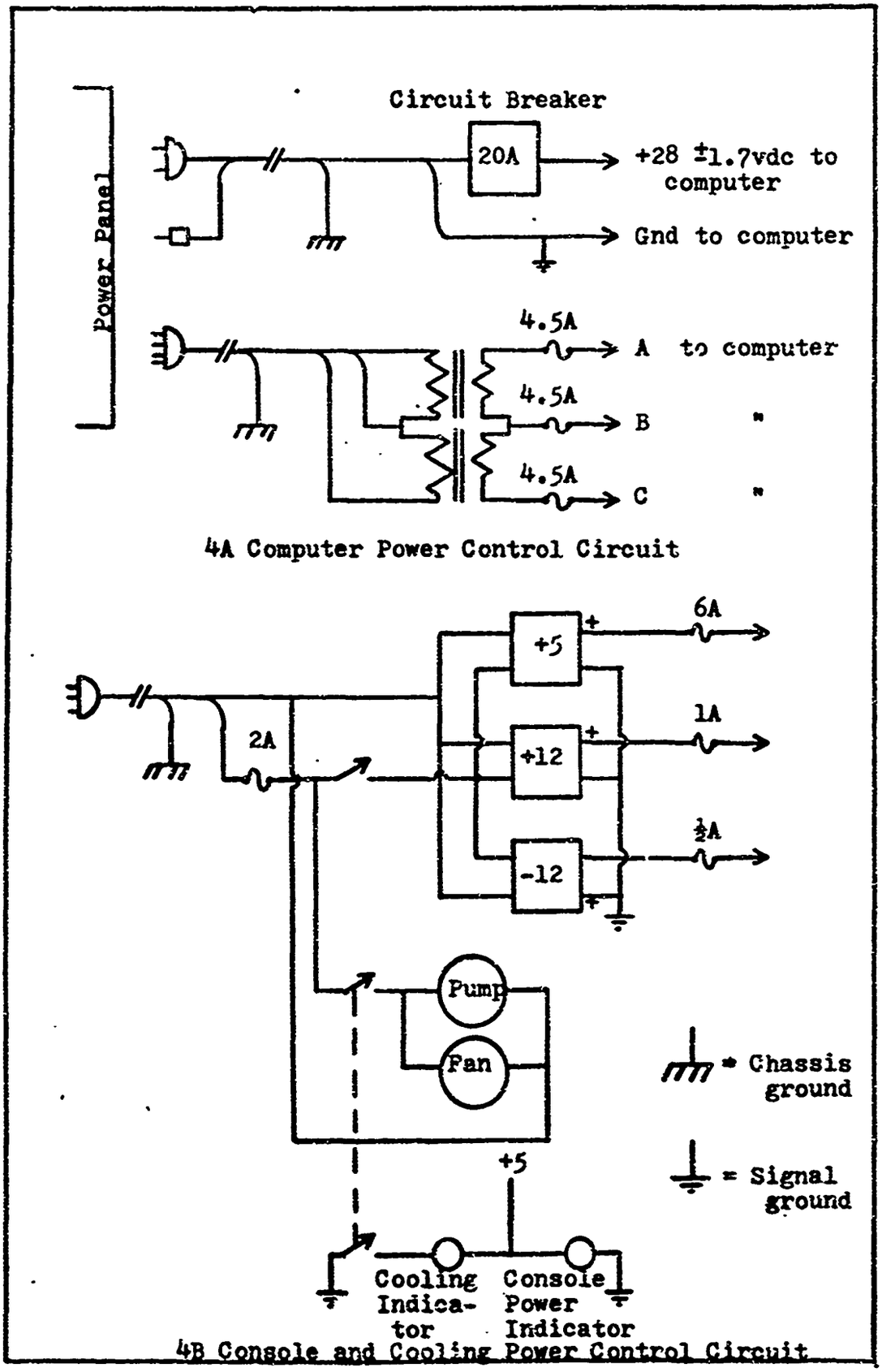


Figure 4. PDU Circuits.

mon power switch.

There are two grounds or commons in the console which are called chassis ground and signal ground. The chassis ground is to prevent shock and other electrical hazards when working with the console. The ground line from the 115v ac source, the panel ground, and the ground wire from the 400Hz alternator are all tied to chassis ground. Neither side of the 115v ac source is tied to either ground. The signal ground acts as a power return for all dc sources and as a common for all signals. The negative side of the +28, +5 and +12vdc sources, and the positive side of the -12vdc supply are tied to signal ground. The two grounds are not intended to be tied together in the console though this may occur with no problem (for instance, another experiment using the power panel may tie the -28vdc to ground).

Power distribution in the console originates at the Power Distribution Unit (PDU). The PDU acts as a patch panel for wiring the power systems and provides a central location for power troubleshooting and power routing. Each circuit board in the console has its own power and signal ground lines running to the PDU. This was done to eliminate some accumulated noise on the power lines and to insure that multiple connections did not reduce the voltages. The PDU is illustrated in Fig. 5.

Cooling System

Specifications. The cooling requirements for the D37C computer are given in the Test and Recycle Specs (Ref 5). The

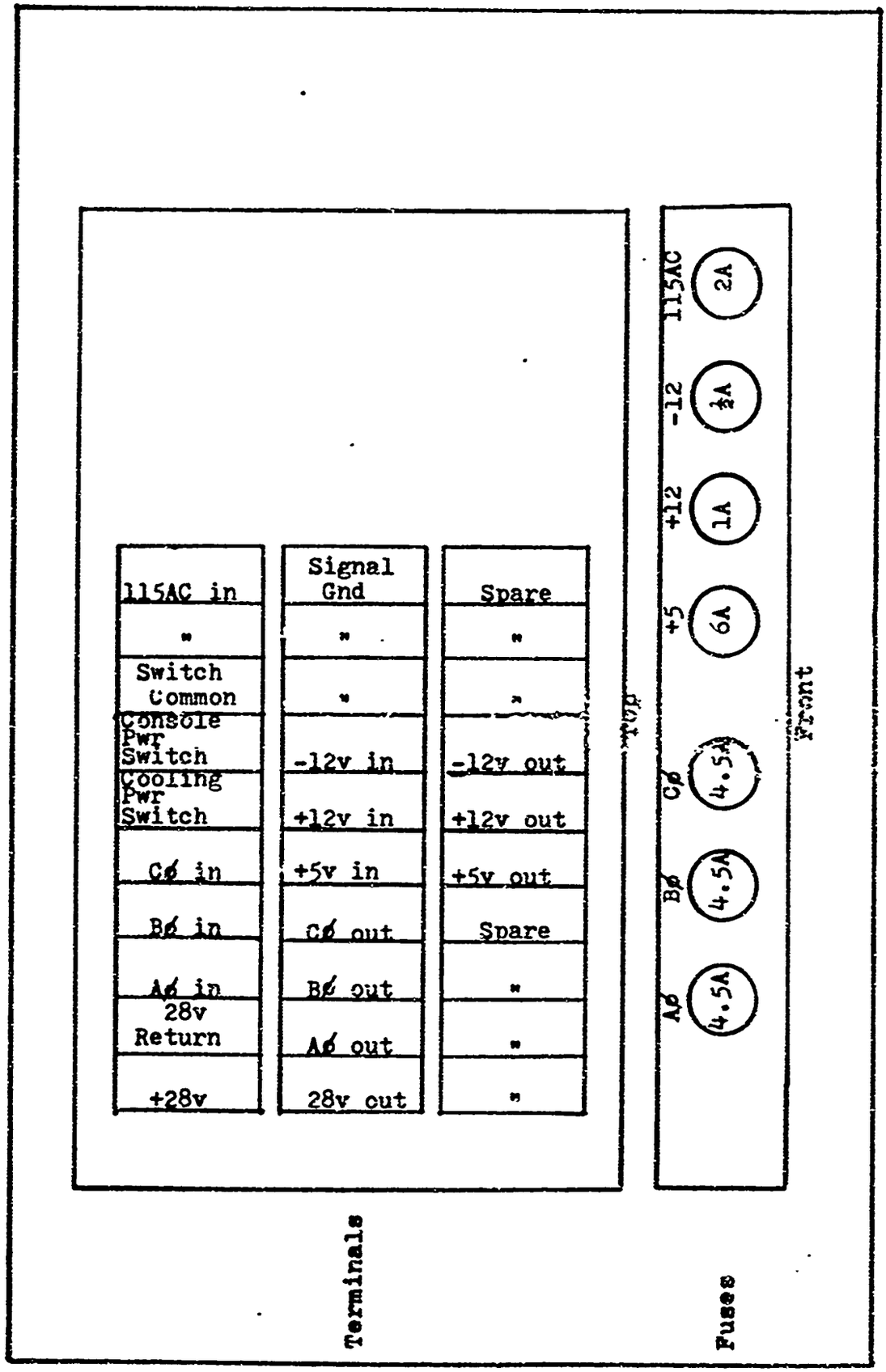


Figure 5. Power Distribution Unit.

computer's electronics are completely enclosed in a metal casing and cooled by coolant circulating through the casing's hollow walls. The liquid coolant is a water solution of .1 to .22 percent by weight of sodium chromate and distilled or deionized water having a minimum specific resistance of 175,000 ohms. The temperature of the water shall be +40 (+10, -5) degrees F at the inlet and +56 (+7, -4) at the outlet and at no time should the outlet temperature exceed 70 degrees F (Ref 5). The cooling system must remove 350 watts of heat dissipated by the computer.

Organization. The mentioned specifications are, as before, designed to simulate a rocket environment for testing purposes. The requirements may have to be relaxed to utilize available equipment. This is feasible as long as a suitable environment for the circuits is maintained. The computer may, in fact, be operated outside the specified temperature range as long as moisture does not form on the inside walls (too cold) or as long as the outlet temperature does not exceed 70°F (Ref 5). Relaxing the cooling requirements results in a wide range of possible solutions including air cooling.

The computer cooling system may consist of any combination of open loop or closed loop systems using either liquid or air heat transport. A refrigeration unit may be used to remove heat from the coolant or the computer itself may be used as an evaporator in a refrigeration cycle. Tap water may keep the computer cool in an open loop system. To keep hard water deposits from clogging the cooling ducts, tap water may be used

to remove heat from a coolant in a combined open and closed loop system. Other cooling systems may include removing the computer covers and forcing air in and around the circuits to cool them directly.

Design. The system selected for cooling the D37C uses forced air and circulating liquid. Since no refrigeration unit or tap-and-drain were available, this system was chosen as the most effective and easiest to implement. The D37C was not designed for air cooling but air can be forced down between the circuit boards and around the IC's. At the same time, distilled water circulates through the walls to lower heat gradients and to cool those parts not sufficiently cooled by air. In this way, the IC's act as their own radiators and are cooled more directly instead of the heat traveling first to the computer walls. This justifies cooling with room temperature air (around 70°F) and allowing the coolant to raise above 70°F. Removing a cover for air cooling, however, increases the possibility of dust and foreign objects entering the casing. Precautions should be taken to keep the insides clean because of the closeness of IC leads and the possibility of foreign object shorts.

Realization. This system was implemented with four "Muffin" fans to circulate the air and a small pump to circulate the liquid (see Fig. 6). The four fans are capable of circulating two to four hundred cubic feet of air per minute. Because obstructions in the casing prohibit flow through air, only one cover was removed. The side of the computer opposite

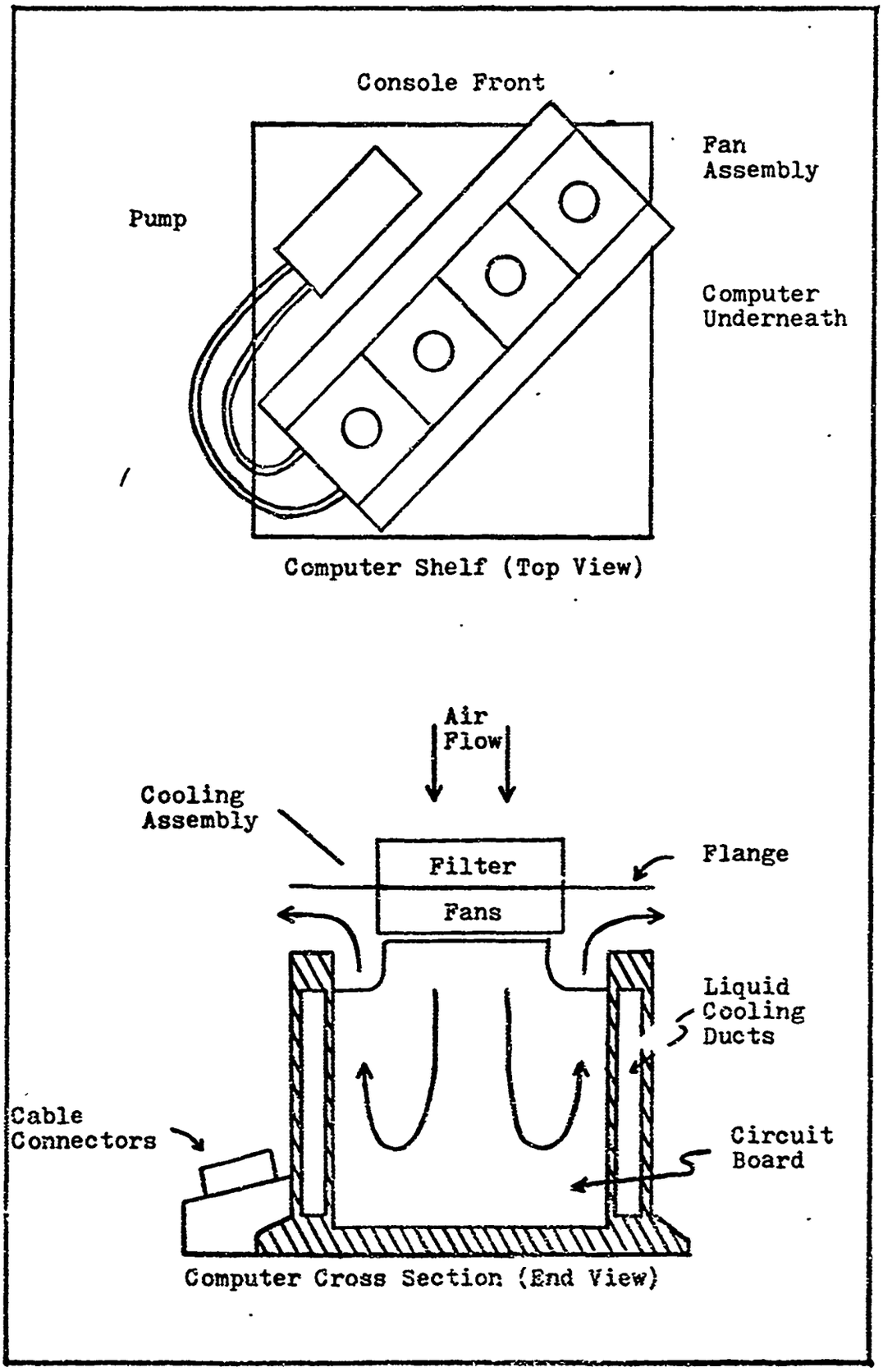


Figure 6. Computer Cooling System.

the cable connectors was removed and the fans, bolted together, were placed over the center of the circuit boards on the card end protectors. This leaves approximately one inch on either side of the fans for exhaust air. Some "horse-hair" packaging material was placed over the fan intakes for crude filtering. Flanges on the fan assembly prevents objects from dropping into the computer housing and acts as a manifold to reduce recirculated air. A pump with two to three gallons per minute capacity was placed on the shelf with the computer and connected with plastic hoses. No special hose connectors are necessary since the friction fit is water tight. The whole system is controlled by a front panel switch as indicated in Fig. 4B.

This system is not sufficient for continuous duty but is the most effective cooling scheme available. The circulating liquid temperature gradually increases when the system is running. When the temperature reaches 100°F (about 20 minutes) the primary power is removed while the system cools or while the liquid is replaced.

Conclusion

Summary. It has been shown that external systems for the D37C computer can be implemented easily. This has been done by supplying the needs of the computer rather than trying to meet the specifications designed to simulate a rocket environment. These mentioned systems are just one solution of many that can be built. Simpler systems and more complex systems are possible. For example, the power circuit may be expanded to an automatic system that shuts off when temperature or vol-

tages get out of tolerances.

There is, presently, an additional constraint for building systems at AFIT. The D37C computer AFIT possesses is classified "secret" due to previous information on the memory disk. It is necessary, therefore, to remove the computer from the console and put it in a safe after each day's use. This means that every system associated with the computer must be easily connected and disconnected. This constraint will not be present when the computers become surplus.

System Interconnection. The external support systems are located in the cabinet as shown in Fig. 7 and electrically interconnected as shown in Fig. 4. The power shelf (bottom) pulls out to provide easy access to the Power Distribution Unit (PDU) and power supplies. The computer shelf also pulls out to allow easy hook up of power, cooling and cables. All switches for power and cooling are located on the front panel.

Recommendations. The following recommendations are made in the interest of improving the system or as experiments to better understand the limits of the machine.

1. Because of the closeness of circuits in the computer there is a chance of foreign object shorts with the present cooling system. It is recommended that the computer be cooled only with a liquid system of continuous duty cycle if the equipment becomes available. Until then, efforts for a better filtering system would increase the present system's reliability by keeping the close circuit leads clean.

2. The power system may be expanded to include con-

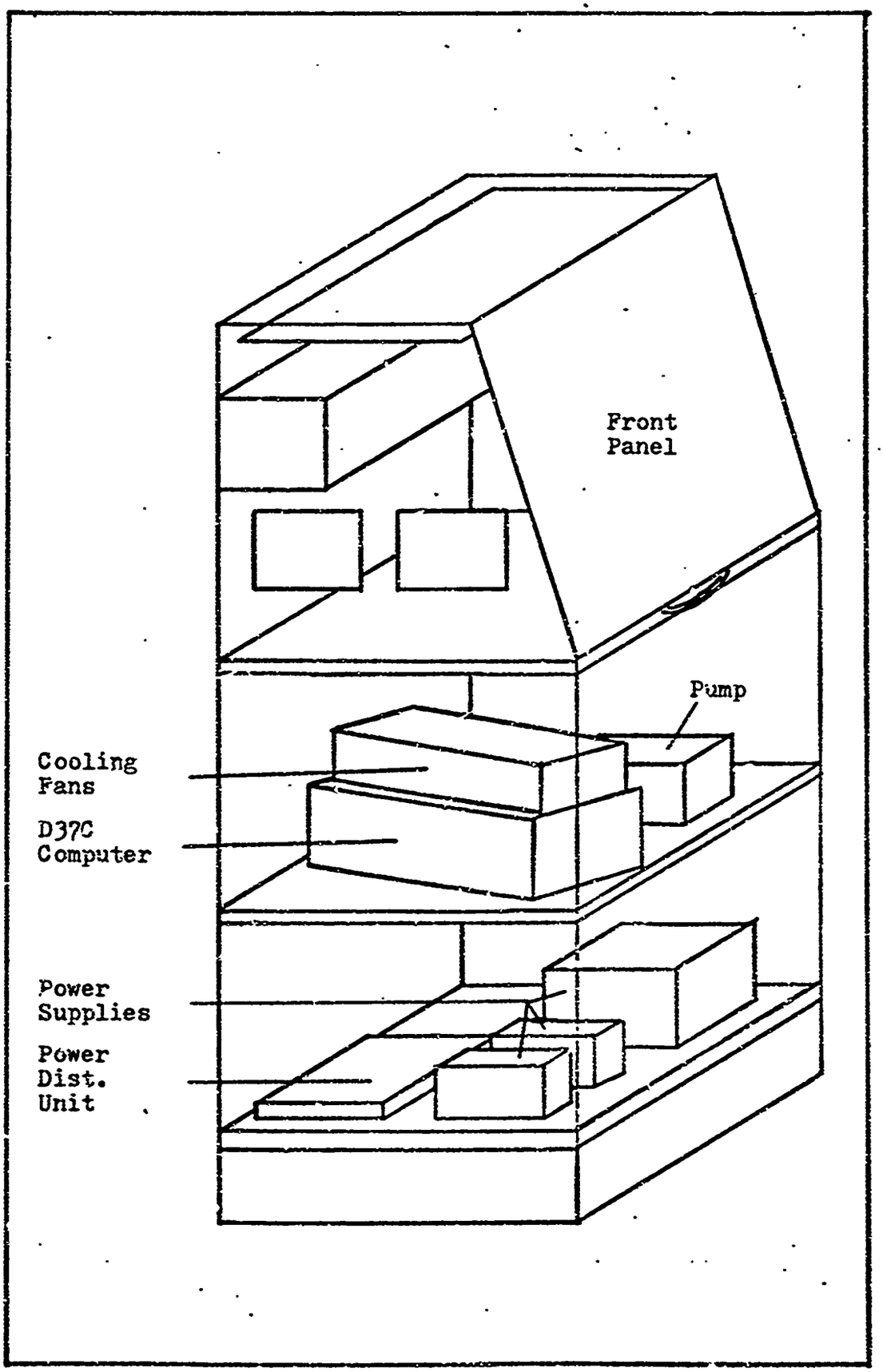


Figure 7. Power and Cooling Systems Locations.

sole switching and automatic monitoring devices. Such a system would add complexity but it may also increase protection from power faults.

3. As an experiment, the speed of the computer could be increased by increasing the frequency of the memory motor power. Since the memory motor is a three phase synchronous motor it can be made to run faster by increasing the power frequency. In turn, since the clock and other timing pulses come from tracks on the disk the whole computer would work faster. Before this is attempted, however, there are many considerations to make. There is some indication in Reference 3 of the electronics being capable of a one mega Hz clock which is almost a three fold increase. The motor, however, is not expected to operate that fast (almost 18000rpm). The reduced motor torque caused by higher frequencies can be offset some by increasing the voltage. However, the bearing wear and disk stresses are unknown at higher speeds. The read and write heads may also be unreliable at higher speeds. In all, the total increase in computer speed cannot be expected to be much over 50%.

III. Control and Monitor Systems

After supplying the computer with proper power and cooling systems, it is necessary to control and monitor its functions before it is suitable for any application. This is done by properly controlling the computers modes and developing a simple memory loading scheme. In order to monitor the computers functions the major modes must be indicated and the contents of selected registers must be displayed. In effect, the monitor and control circuits provide simple I/O for the computer which alone may be sufficient for many applications. The monitor and control systems fit into the total system as shown in Fig. 8.

Interfacing

Interfacing the computer's signals, matches voltage levels, impedances, and current requirements to the external (TTL) logic circuits. This is necessary because the external logic is realized from TTL small and medium scale integrated circuits. These circuits were used instead of building compatible discrete logic because they were available, easy to design with, came in logic "blocks" of several gates per chip, and have relatively high noise immunity. Most computer signals vary from -15 to +12 volts and are therefore incompatible with the 0 to +5 voltage levels of TTL logic. Nearly all of the signals, both input and output, may be interfaced by using line drivers and line receivers in IC form. Some require operational amplifier circuits and others need inverters to con-

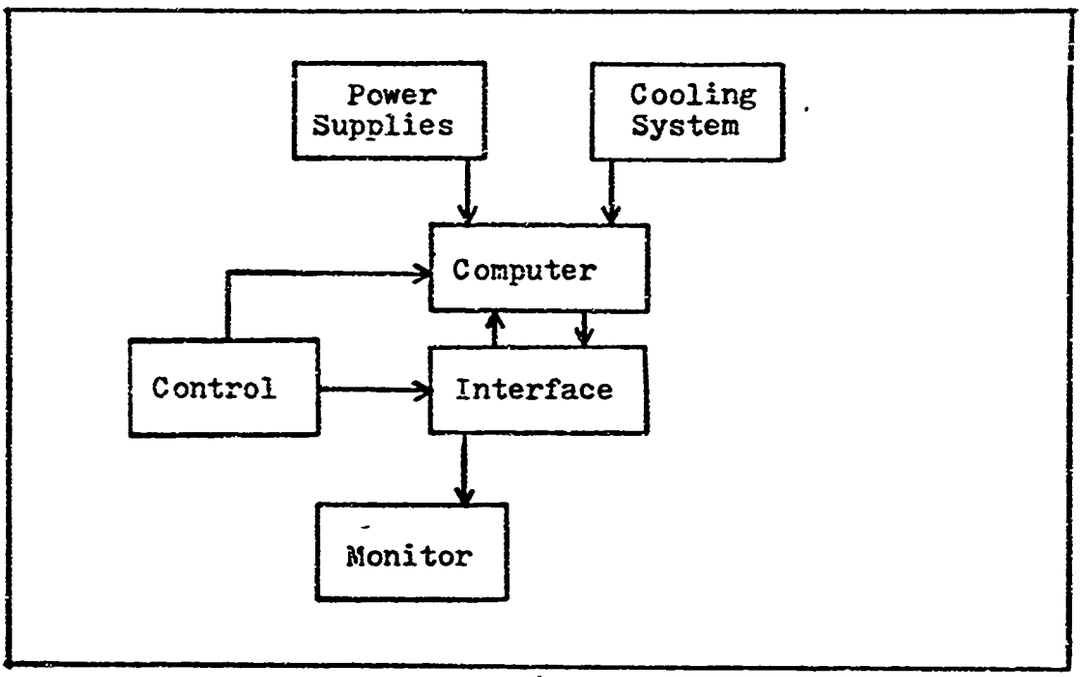


Figure 8. System Block Diagram.

vert from negative to positive logic.

The following investigation will indicate if a signal has to be interfaced or if it is compatible with the circuit. For a complete listing of interfaced signals and schematics see Appendix B.

Mode Control and Monitor

Controlling and monitoring the computers modes of operation requires some very simple circuits. It is necessary, however, to have some understanding of the modes and how the computer functions (Ref 5, 11, and 3).

Major Modes. The computer can operate in several modes and submodes which are of particular interest to the operator/programmer. These modes, with descriptions, are listed below:

i) Compute Mode - While in this mode the computer exe-

cutes an internally stored program.

1a) Single Cycle Submode - In this submode, the computer executes one stored instruction.

2) Noncompute Mode; Load - In this mode the computer is capable of receiving information on the character input lines (Ref 5). This mode and the character lines are used for program loading and are discussed later.

2a) Fill Submode - This is a submode of the above Noncompute, Load Mode and is the mode which information may be entered into the computer memory.

2b) Verify Submode - In this mode the contents of computer memory may be verified (or compared) against information on the character input lines.

3) Noncompute Mode; Nonload - The noncompute-nonload mode is defined by the following major submodes.

3a) Sync Submode - In this mode the computer's electronic section is brought into synchronization with the rotating disk memory. This is done by synchronizing the bit counter with the sector track (see Appendix A).

3b) Manual Halt Submode - In this mode the computer is in a wait state.

3c) Program Halt Submode - This mode is entered from the compute mode by an executed instruction. In this mode the computer is in another wait state.

3d) Conditional Fill Submode - This mode provides a security precaution to prohibit unauthorized personnel from loading the computer memory. It prohibits entry into the

fill submode unless the first four words entered agree with the first four words of channel 12, bank 0.

4) Interruption and Recovery Mode - During this mode the computer, upon detection of a simulated transient disturbance, will interrupt normal operations, enter a dormant state, and then recover to the same program location.

Specifications and Organization. It is desired to have some control over the computer's transitions between modes and to have some indication of the current operating mode.

Two of the modes serve little use in general purpose applications and are therefore eliminated or disabled. These modes are the conditional fill submode and the interruption and recovery mode. For most applications the security facet of the conditional fill mode is not needed and only serves to hinder the entrance into fill mode. The conditional fill mode may be bypassed by enabling the Fsc line and applying a true signal. The line is enabled by making an electrical connection on Logic No. 10, connector J216, between test points B36 and B32 (Ref 5). Once this is done the fill mode may be entered directly by applying a true (-4 to -24 vdc) to Fsc. The interrupt and recover mode forces the computer into a dormant state (all internal power supplies disabled) which would have little use in most applications. The interrupt mode may be avoided by not programming a simulated random dump (SRD) instruction and applying a false signal to the Idt input term. A false for the Idt term is +12±8 vdc input or an open circuit (Ref 5). Controlling the remaining modes is necessary

for effective computer control.

The sync mode must be entered each time the machine is turned on in order to synchronize the computer. The sync mode is entered by applying a true signal on the master reset line (Mrc) for a minimum of 55 μsec after the memory has reached synchronous speed. A true for Mrc is -15 (+11,-12) vdc and a false is +12±8 vdc or an open circuit. The computer automatically exits the sync mode to the manual halt mode (Ref 5).

The compute mode is entered only from the manual halt mode in one of two ways. Normal execution is started by changing the halt prime (Khc') input signal from false to true for at least 200 microseconds. Halt prime may then return to false. The single cycle prime (Ksk') input signal remains true throughout the sequence. The compute mode may also be entered for the execution of one instruction and then returned to manual halt by the initiation of the single cycle sequence. This sequence calls for Ksk' to change from true to false then Khc' is changed to true for at least 200 microseconds. Then Khc' returns to false and Ksk' returns to true (Ref 5). Timing diagrams for both of these sequences and voltage levels for the signals are given in Fig. 9.

As mentioned earlier, a true signal on the Fsc line will put the computer into noncompute-load mode from either the manual halt or program halt modes. Once in this mode, character inputs to the computer may be made as described in the Program Load section of this chapter. The character inputs can change the computer modes as well as load the memory.

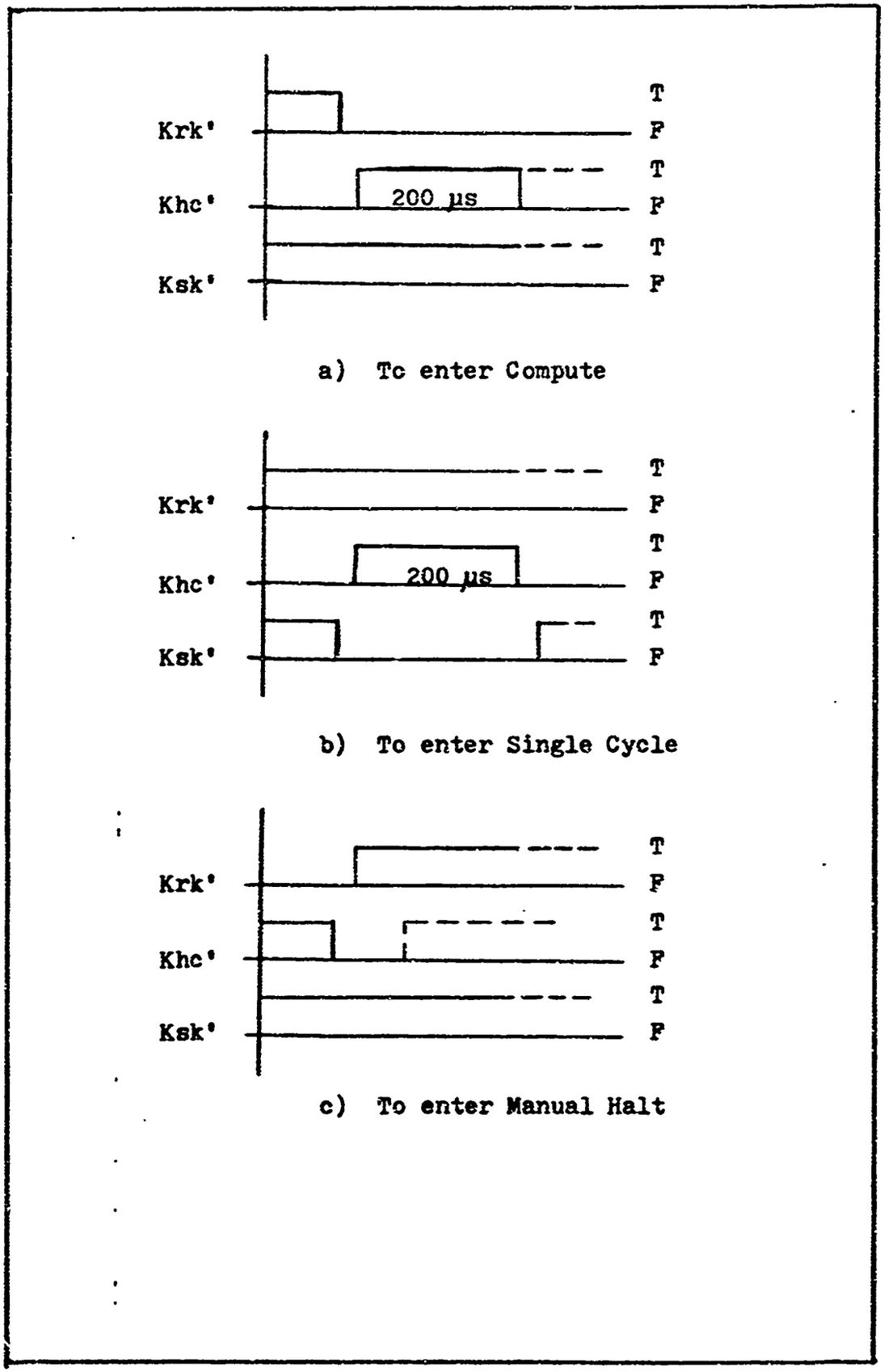


Figure 9. Timing Sequences for Mode Control.

Commands can be given to change from the fill submode to the verify submode or from verify to fill. A compute command removes the computer from noncompute-load and enters it into manual halt. A halt command changes it to program halt (Ref 5).

The manual halt submode may be entered several ways. It may be entered from compute by the single cycle sequence already mentioned or by the following sequence of inputs. Initially the halt prime (Khc') signal changes to a quiescent false state. Tnen run prime (Krk') changes from false to true. The single cycle prime (Ksk') signal will remain true throughout the sequence, see Fig. 9 (Ref 5). This same signal sequence will enter the computer into manual halt from program halt. Manual halt may also be entered from load mode by a compute command, as mentioned in the preceeding paragraph, or by a parity or verify error (see program load section). Exit from the manual halt mode may be to compute or noncompute-load by methods already described.

The program halt submode may be entered in one of two ways. One is by a halt instruction executed while in compute. The other way is by a halt command entered while in noncompute-load mode. The computer will return to the load mode given a true Fsc term. It may also leave program halt and enter manual halt by the sequence of instructions already described in the paragraph on the manual halt mode.

The state diagram in Fig. 10 illustrates the possible state changes and how they are made. It should be noted that entry into the noncompute-load mode does not insure entry into

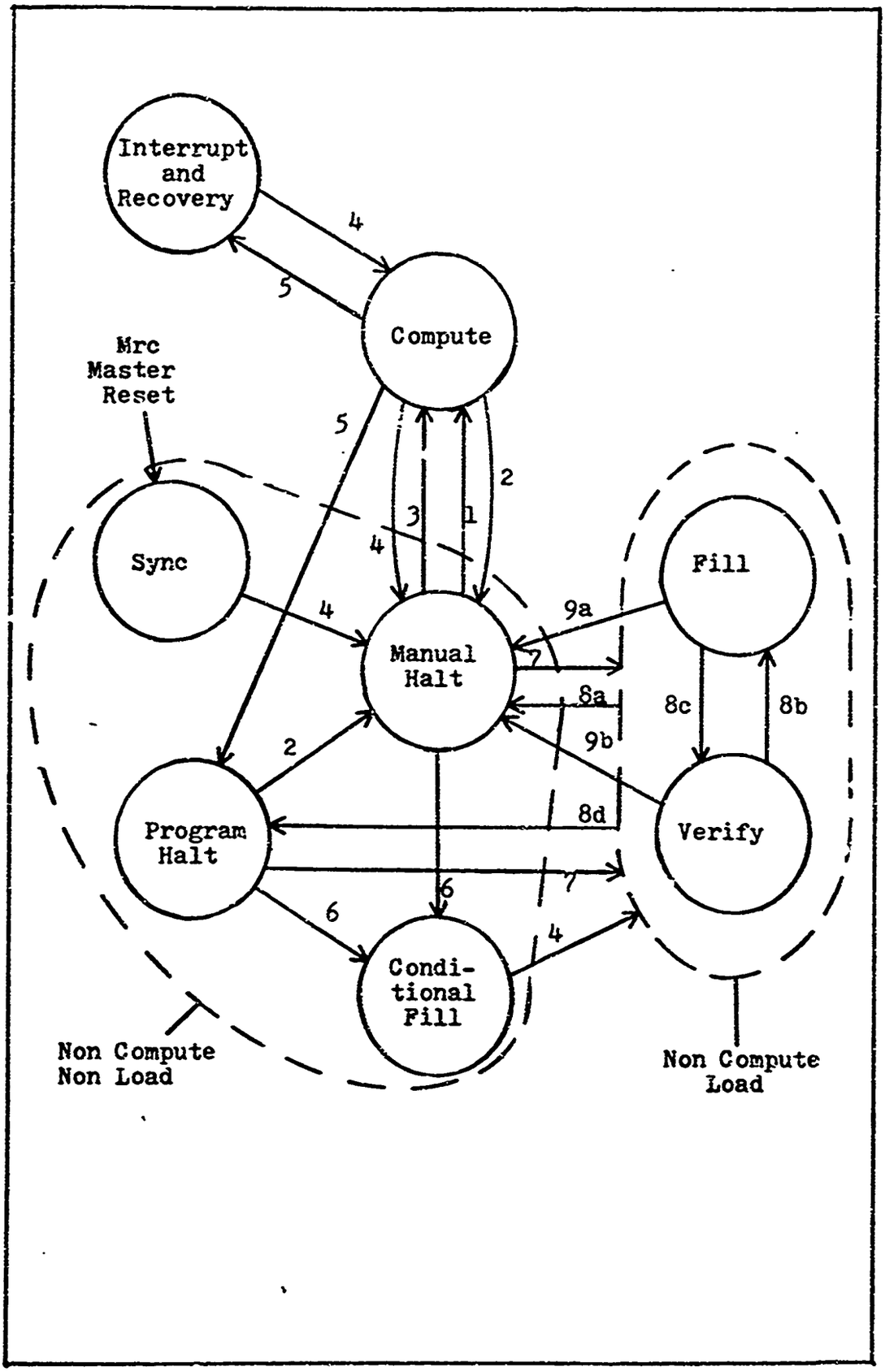


Figure 10. State Transition Diagram for Major Modes. (page 1 of 2)

1 - Initiated by sequence in Fig. 9a

2 - Initiated by sequence in Fig. 9c

3 - Initiated by sequence in Fig. 9b

4 - Automatic or computer controlled transistion

5 - Initiated from execution of store instruction

6 - Initiated when Fsc = F and a character is presented on the character input lines

7 - Initiated when Fsc = T

8 - Character input commands
- a - Compute
- b - Fill
- c - Verify
- d - Halt

9 - Initiated by error condition
- a - Parity
- b - Verify

Figure 10. State Transition Diagram for Major Modes. (page 2 of 2)

the fill submode, although, this is usually the case.

There are several output signals from the computer available to indicate its current operating mode. The modes and and corresponding signal states are listed in Table II (Ref 5). The terms circled are those that will be used to indicate the computer's mode. One exception to this is the sync mode. The Syt' term is false when the computer is synchronized and true when it is not, so this term will be monitored as a warning against non-synchronization and not as an indicator of the sync mode. This will better serve the operator/programmer since non-synchronization prohibits proper operation.

Design and Realization. There are at least two alternatives in supplying appropriate switch and circuit combinations which allow an operator to control and monitor the computer's modes. One is to supply a button for each mode and submode, thereby allowing selection of any mode by pressing a single button. This method would require complicated sequential circuits that would initiate proper signal changes and mode transitions. For example, to enter the computer into program halt from compute by pressing a button, the computer would first have to go to manual halt, then load mode, and finally program halt. A simpler method of providing mode control assumes the operator has some knowledge of allowable mode transitions and provides input signal control with minimal logic. This method is similar in design to that used on the D17B console at AFIT. Using this method, therefore, provides simple control circuits and switches with functions that are

Table II.
Mode Monitor Signal States

Mode	Submode	Kc	Kt'	Lkc	Nmhk	03k	Phk	Pk	Pvec	Pvk	Syt'
Compute		(T)	F	F	F	U	F	F	F	F	F
Non Compute Load	Fill	F	T	(T)	F	(F)	F	F	F	F	F
	Verify	F	T	(T)	F	(T)	F	F	F	F	F
Non Compute Non Load	Sync	F	T	F	F	U	F	F	F	F	tg
	Man Halt	F	T	F	(T)	U	F	F	F	F	F
	MH + PE	F	T	F	(T)	U	F	(T)	T	F	F
	MH + VE	F	T	F	(T)	U	F	F	T	(T)	F
	Prog Halt	F	T	F	F	U	(T)	F	F	F	F
	Cond Fill	F	T	F	F	F	F	F	F	F	F
Interrupt and Recovery		U ⟶									

T = True
F = False
U = Undefined
tg = toggling

Kc = Compute mode
Kt' = Compute prime
Lkc = Load mode
Nmhk = Manual Halt mode
03k = Verify Submode
Phk = Program Halt mode

Pk = Parity error
Pvec = Parity or verify error
Pvk = Verify error
Syt' = Sync prime
MH + PE = Manual Halt from Parity Error
MH + VE = Manual Halt from Verify Error

already familiar to the personnel in AFIT's minuteman laboratory.

The simplest of the mode control circuits provide levels for the Mrc and Fsc lines which controls entrance into sync submode and noncompute-load mode, respectively. Momentary contact pushbuttons are used to supply a -12±1 vdc, or True level, on the line when pressed, and an open circuit, or False level, when released. These switches will be labelled MASTER RESET for the Mrc term and INITIATE LOAD for the Fsc term. The schematic is shown in Fig. 11.

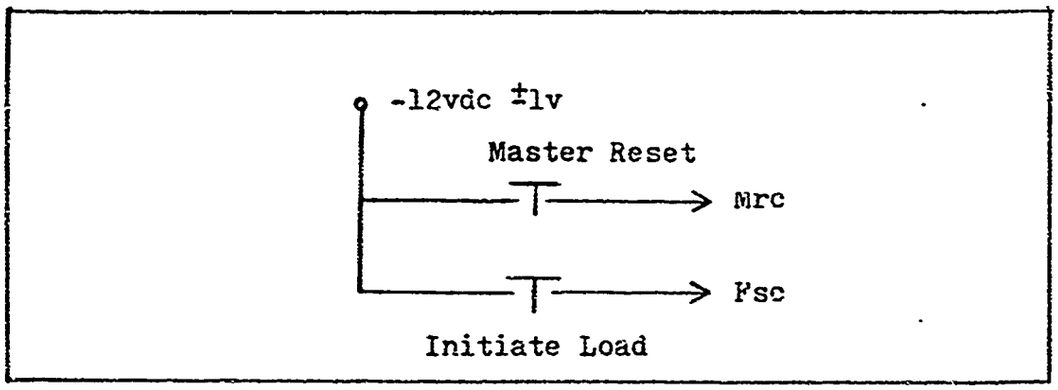


Figure 11. Master Reset and Initiate Load.

Entrance into the single cycle, compute, and manual halt modes is controlled by two switches labelled RUN/HALT and SINGLE CYCLE. These switches are debounced and combined with a monostable multivibrator to generate the proper sequencing (see Fig. 9) for the KsK', Khc', and KrK' terms. Debouncing is required to prohibit multiple triggering and the monostable provides the proper pulse width for Khc'. The KsK', Khc', and KrK' terms are interfaced and at TTL levels they are called SS', Hlt', and Rn', respectively. The schematics for these circuits are shown in Fig. 12. Note that the SS term is inver-

ted at the interfacing circuits.

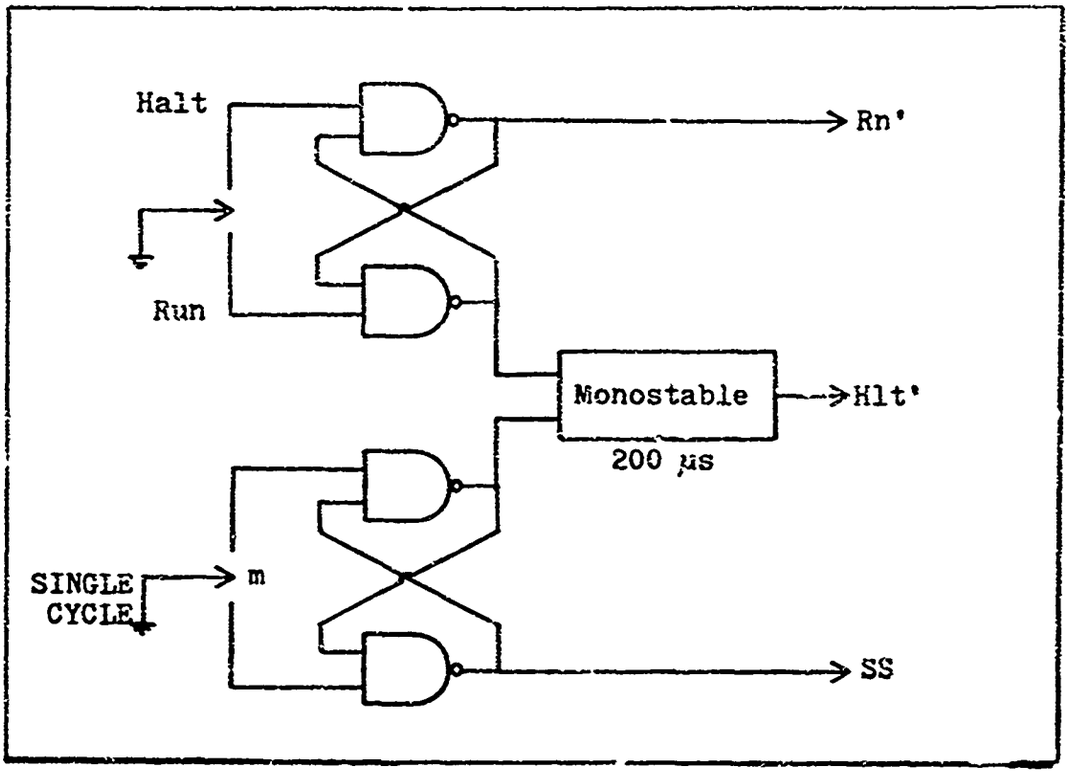


Figure 12. Mode Control Circuit.

Of the remaining modes, program halt, fill, and verify will be controlled by an internally stored program or by the character inputs, which will be discussed in the section on Program Loading.

The mode indicators are driven by the signals referred to by the circled states on Table II. Except for interfacing and inverting, the only modes that require logic circuits are fill and verify. The following boolean formulas can be taken directly from the table.

Fill = LKc · 03K' Verify = LKc · 03K

The schematics for these and all other modes and error indicators are shown in Fig. 13. Note that open collector gates

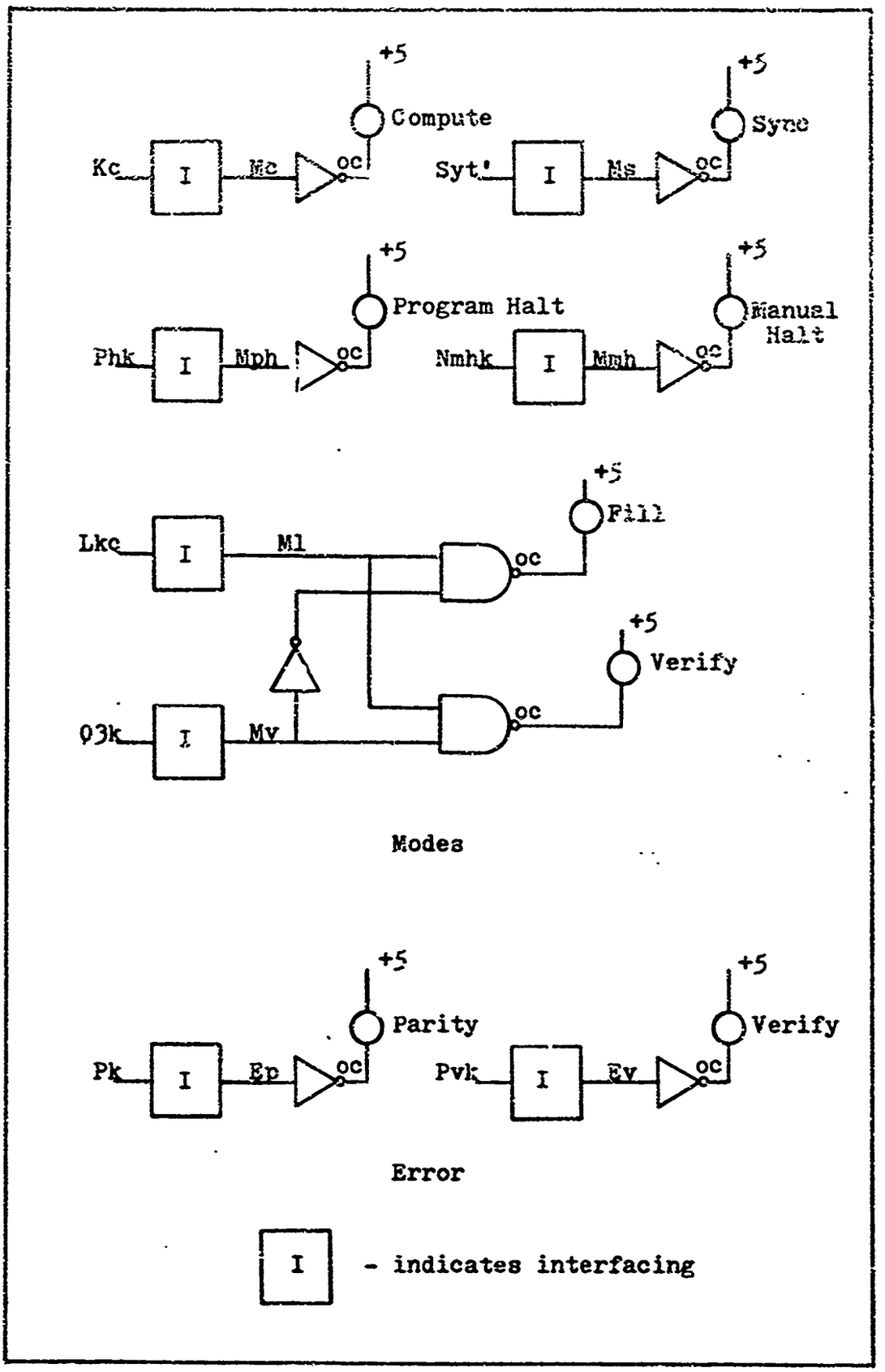


Figure 13. Mode and Error Indicators.

are used to drive the lamps.

Program Loading

Once a method is devised to control the particular operating modes of the machine it is necessary to have some way of programming it. There are several ways to input information into the computer memory while it is in the compute mode, but these are not useful for initial start up if there is not some kind of software loader already present. Therefore, this section will develop the circuits necessary to input information on the character input lines which are activated in the non-compute-load mode.

Specification and Organization. The character inputs were designed to load the memory from a paper tape reader or similar device. The computer can accept five bit characters up to 800 per second. The characters consist of four information bits plus one odd parity bit. The character codes represent the octal digits and commands listed in Table III. When the octal codes are entered, the contents of the Lower Accumulator are shifted to the left three bits and the octal digit is entered in the rightmost three bits. The control commands have the following functions. The "Halt" command enters the computer into the program halt mode. "Location" command enters the contents of the Lower Accumulator into the Instruction register. "Fill" and "Verify" enters the computer into those respective submodes. "Compute" enters the computer into manual halt mode. "Enter" enters (or compares, if in verify submode) the contents of the Lower Accumulator into

Table III.

Character Input Codes

Octal Numbers	I5	I4	I3	I2	I1
0	1	0	0	0	0
1	0	0	0	0	1
2	0	0	0	1	0
3	1	0	0	1	1
4	0	0	1	0	0
5	1	0	1	0	1
6	1	0	1	1	0
7	0	0	1	1	1
Control Commands					
Halt	0	1	0	0	0
Location	1	1	0	0	1
Fill	1	1	0	1	0
Verify	0	1	0	1	1
Compute	1	1	1	0	0
Enter	0	1	1	0	1
Clear	0	1	1	1	0
Delete	1	1	1	1	1

(with) the memory location specified by the contents of the Instruction register. The Instruction register is then incremented. "Clear" clears the Lower Accumulator. Finally "Delete" erases or deletes the last code entered. The codes are entered on five lines labelled I1c through I5c and are clocked in by the terms Tc and Tc'. Input signal Tc is used to clock in signals with switch bounce and Tc' is used for a bounceless source (Ref 5, 27). In either case the character lines must be stable prior to or within 10 microseconds after the clock changes. Then all must remain stationary for a minimum of 150 microseconds. The transition time of all signals is immaterial.

An additional signal is necessary to load the cold channels of memory. The write enable signal, Ewc, must be true (+22 - +39 vdc) to write in the cold channels. if this signal is false (open circuit) at shut down, the information in cold storage will be saved for the next start.

Design and Realization. It is possible to input the characters with five switches for the code and a button to enter it. This method, however, makes programming a long and tedious process. It is also very susceptible to human error since five separate switches must be set for each character. Because of this handicap it is better to sacrifice some circuit simplicity to aid the programmer. By using a keyboard and some logic, a character can be entered by pressing one button, thereby speeding the operation and making it more reliable. Because the logic is used, all the signals must be

interfaced.

Besides loading from the console keyboard it may be desired to add other peripherals to the character inputs. For this reason, the character and clock lines are bus structured using negative logic and wired ANDing.

The schematic for the character input circuit including the WRITE ENABLE switch is shown in Fig. 14. The TTL level signals I1 - I5 represent the I1c - I5c computer terms. The D1 - D5 terms are five data bus lines. The character enter signal, Che, represent the bus for Tc. The five NAND gates act as negative logic OR gates to generate the proper bit pattern. The five lines are then ORed together to sense when to generate an enter, or clock signal. The first monostable delays the clock approximately three milliseconds to avoid any switch bounce. The second monostable then generates a 200 (150 minimum) microsecond clock pulse. The following gate insures that no clock pulses are generated from bounces when the switch is released. The delayed clock pulse slows the rate at which characters may be entered from the keyboard, but it is still much faster than one can type (160 characters per second).

Register Display

Loading a program into the computer is useful only if results can be seen. It would also be helpful for programming and debugging if certain registers can be displayed. This section develops circuits for displaying selected memory registers or locations.

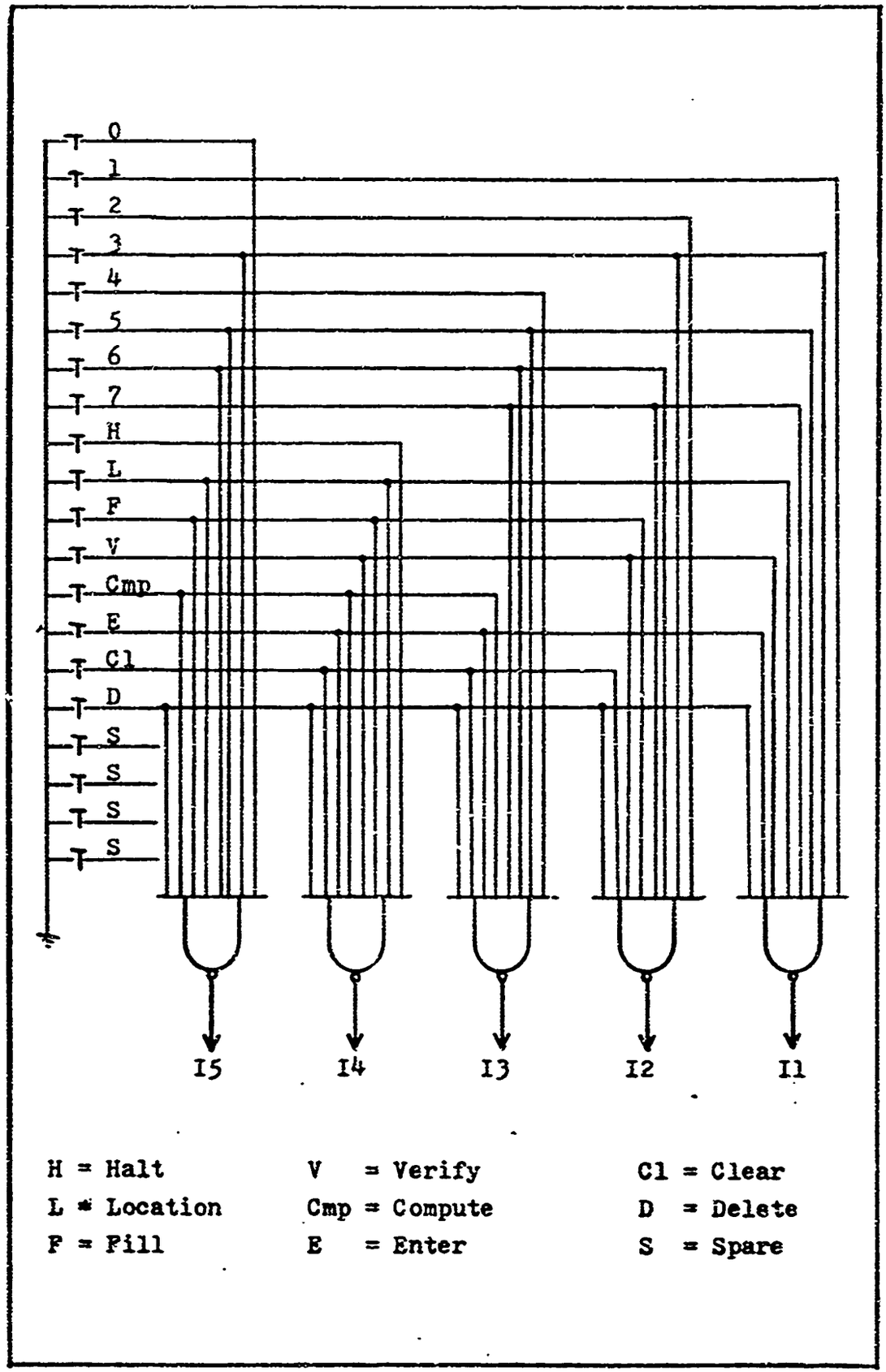


Figure 14. Program Load Circuit. (page 1 of 2)

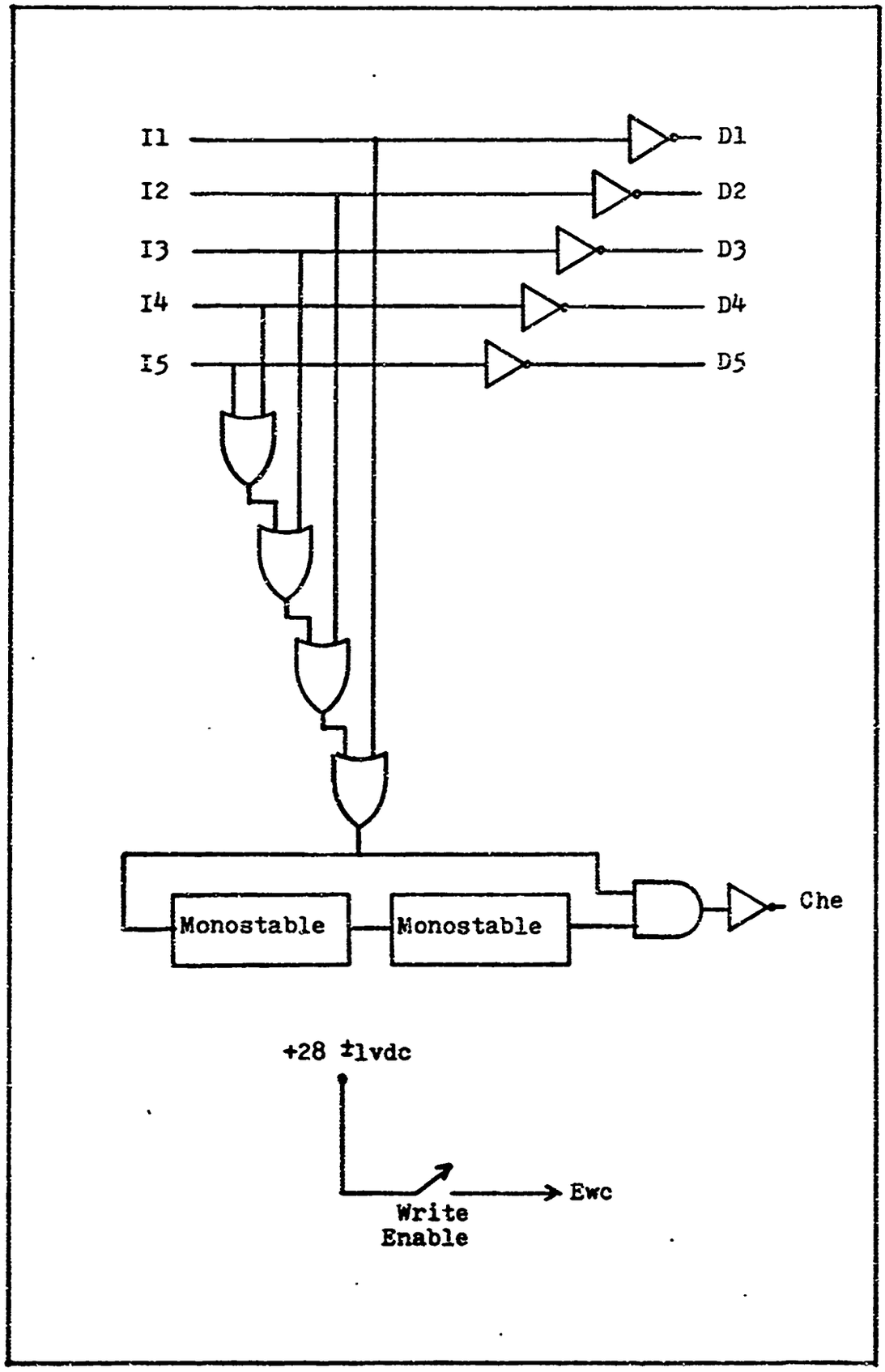


Figure 14. Program Load Circuit. (page 2 of 2)

Specification and Organization. There are several computer signals available for displaying register contents. They are the channel display, Mpx, word rate, Tx, sector track, Sk, clock monitor, Ck, channel display select, Cu0-Cu4, and C10-C14, and the memory bank indicators, B01, B02, BP1, BP2 (Ref 3). These signals are listed and described below:

1) The channel display, Mpx, outputs the entire contents of a selected channel in serial fashion and delayed one bit time. The channel displayed is selected by the channel display select lines.

2) Word rate signal, Tx, is true during the Tx bit time and false at all other times. It is used for timing purposes.

3) The sector track output, Sk, is the serial output of the sector channel. This channel has a sector address in each sector corresponding to the following sector location (see Appendix A).

4) The clock monitor, Ck, is an output of the computer's master clock.

5) The channel display select lines select the channel to be displayed on Mpx. The ten lines are grouped into five upper and five lower signals. Only one from each group may be true at a time. The signal states and selected channel are shown in Fig. 15.

6) The memory bank indicators show which of four banks is used for instruction search and which is used for operand search. The following table illustrates the signals

INPUT	C10	C11	C12	C13	C14
Cu0	S	I	L	A	N
Cu1	Mx	My	Npl	Np2	R
Cu2	F	E	SF3	G	V
Cu3	C	SF2	H	SF1	W
Cu4	U	Y	Ipl	Ip2	

Definitions

S	Sector Track	SF3	One Word Inverted Loop
I	Instruction Register	G	Four word rapid access
L	Lower Accumulator	V	" " " "
A	Accumulator	C	" " " "
N	Number Register	SF2	One Word Inverted Loop
Mx	Hot Channel	H	Sixteen Word
My	" "	SF1	One Word Inverted Loop
Npl	Operand Channel 1	W	" " rapid access
Np2	" " 2	U	" " " "
R	Four word rapid access	Y	Four " " "
F	" " " "	Ipl	Instruction Channel 1
E	Eight " " "	Ip2	" " 2

Figure 15. Channel Display Select.

significance.

Table IV.
Bank Monitor Signal States

BP1	BP2	Program Bank	B01	B02	Operand Bank
F	F	0	F	F	0
F	T	1	F	T	1
T	F	2	T	F	2
T	T	3	T	T	3

The aforementioned computer signals are sufficient for displaying any sector of the available channels and memory banks utilized.

Design. The operator must have a method of controlling the display. Therefore, control will be through the use of five octal thumbwheel switches on the front console. The first (leftmost) switch will be for the upper channel select and the second will be for the lower. The remaining switches will be used to select a single sector of a channel to be displayed. The switches output binary code which is appropriate for the sector select but must be decoded for the channel select.

For the Mpx signal to be useful for display, it must be enabled and latched at the proper instant when the desired sector information is available. The Mpx signal is easily enabled by electrically connecting pins 1 and 2 on interface connector J9 (Ref 5). The latching of Mpx is more difficult. There are several steps involved in deciding when to shift

the Mpx output into a 24 bit register and when to stop the shift. A flowchart of the logic process is shown in Fig. 16. The first step is to latch bits T2 through T8 of the sector track, which indicates the address of the following sector. These bits must then be compared to the sector select switches for coincidence. If it does not occur, the first step is repeated. If coincidence occurs Mpx is shifted into the register, starting at the next Tx time. The following Tx time stops the shift with the desired memory word in the shift register. Fig. 17 is a timing diagram indicating when each step should occur.

In order to eliminate the possibility of "races" in the circuits the computer clock is modified to produce the system clock, Ct. These races are possible because some signals used, such as Tx and Sk, change state at the same time of the clock, and also, additional delays may be introduced in the interfacing circuitry. The modification involves fabricating a clock pulse which lies inside the computer's clock envelope. A leading edge delay of .5 microseconds (approximately 25 gate times) insures proper information at flip-flop inputs before clocking. An advanced negative transition of .4 microseconds (approximately 20 gate times) insures input information does not change on master-slave flip-flops before clocking. See timing diagram in Fig. 18 for graphic explanation.

Realization. All the circuits for this section are realized with transistor-transistor logic, therefore all of the signals must be interfaced to computer voltage levels.

The channel select circuits are simple decoders as shown

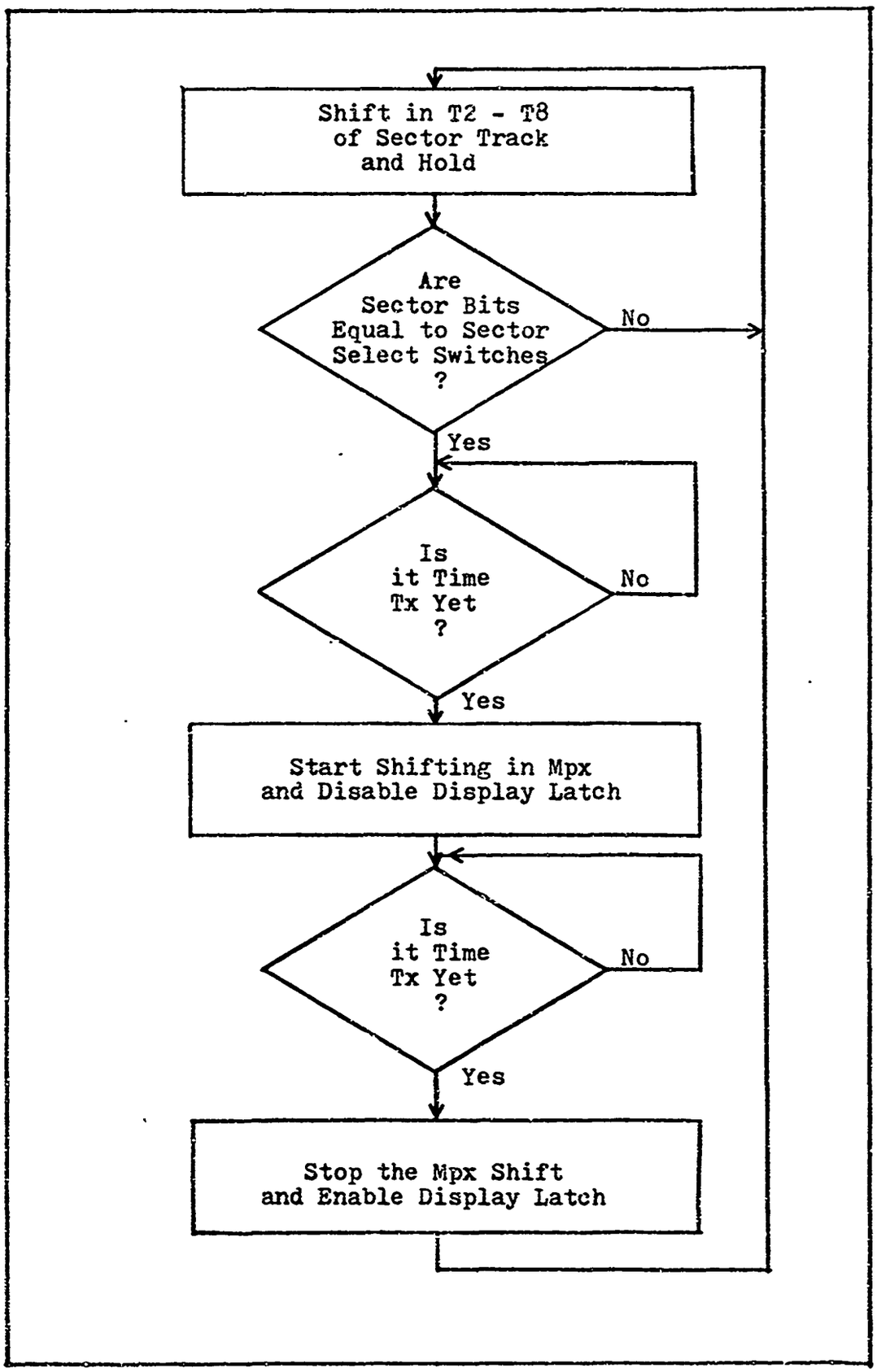
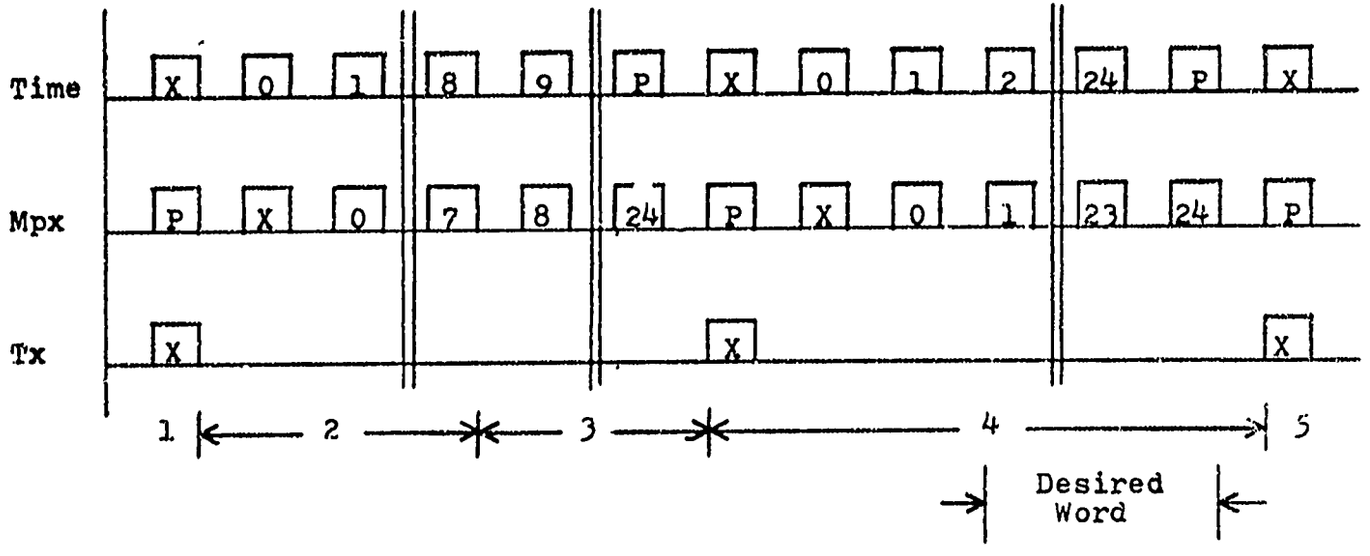


Figure 16. Logical Flow Chart for Register Display.



1) System reset
2) Sector information shifted in
3) Check for coincidence of sector information and sector select switches
4) Mpx is shifted into register
5) Shift stops and system is reset

Figure 17. Display Timing Diagram.

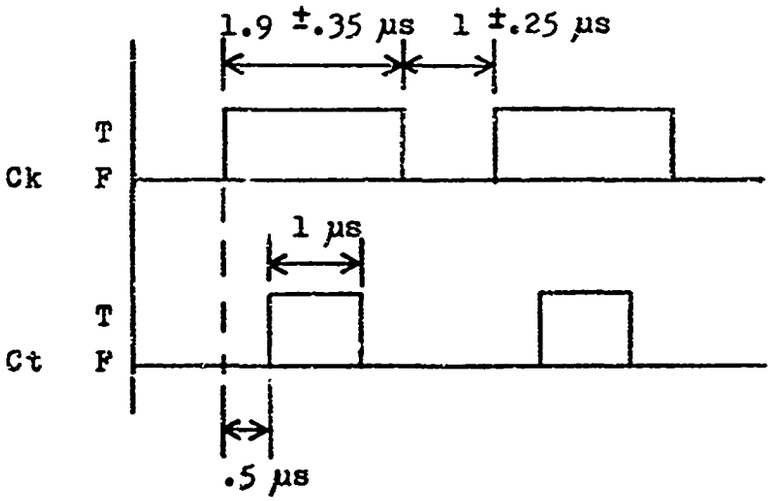


Figure 18. System Clock Timing.

in Fig. 19. Two of these circuits are needed, one for upper channel select signals, and one for the lower. The negative logic outputs are converted to positive levels in the interface circuitry.

The Mpx shift and latch timing circuit is illustrated in Fig. 20. The four-bit counter controls the shifting of sector track information. Nine bits from Tx are shifted in and compared with the sector select switches through two 4 bit magnitude comparitors. If coincidence occurs the flip-flop is set at the leading edge of the next Tx pulse and is reset on the following Tx. The flip-flop gates the system clock to generate the SHIFT signal for the Mpx shift register.

The Mpx shift register and display are shown in Fig. 21. The register is a 24 bit shift register controlled by the preceding timing circuit. The display consists of eight, seven-segment, LED displays with decoding and memory. Twenty-four individual lights may be used but the LED lights were available, and are easier to read since each displays an octal digit. The latching signal (Q' from the timing flip-flop) may be eliminated since the resulting "flicker" would occur less than one percent of the time for durations of about 80 microseconds. The flicker would be totally undetectable with the eye.

The bank indicators illustrated in Fig. 22 use the same LED displays. Since the displays contain decoding circuits the interfaced signals may be wired directly.

The clock schematic is Fig. 23. The first monostable

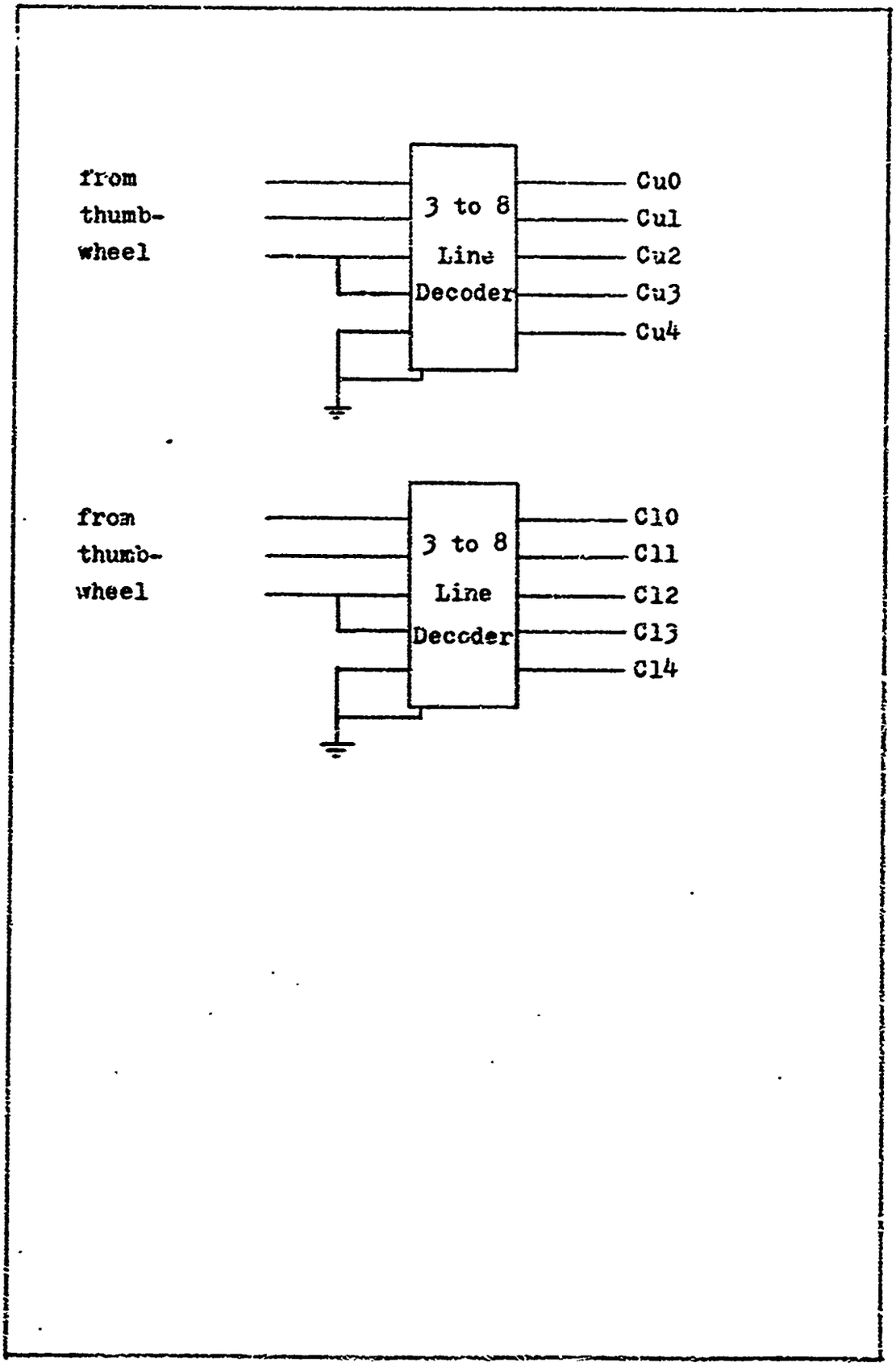


Figure 19. Channel Display Select.

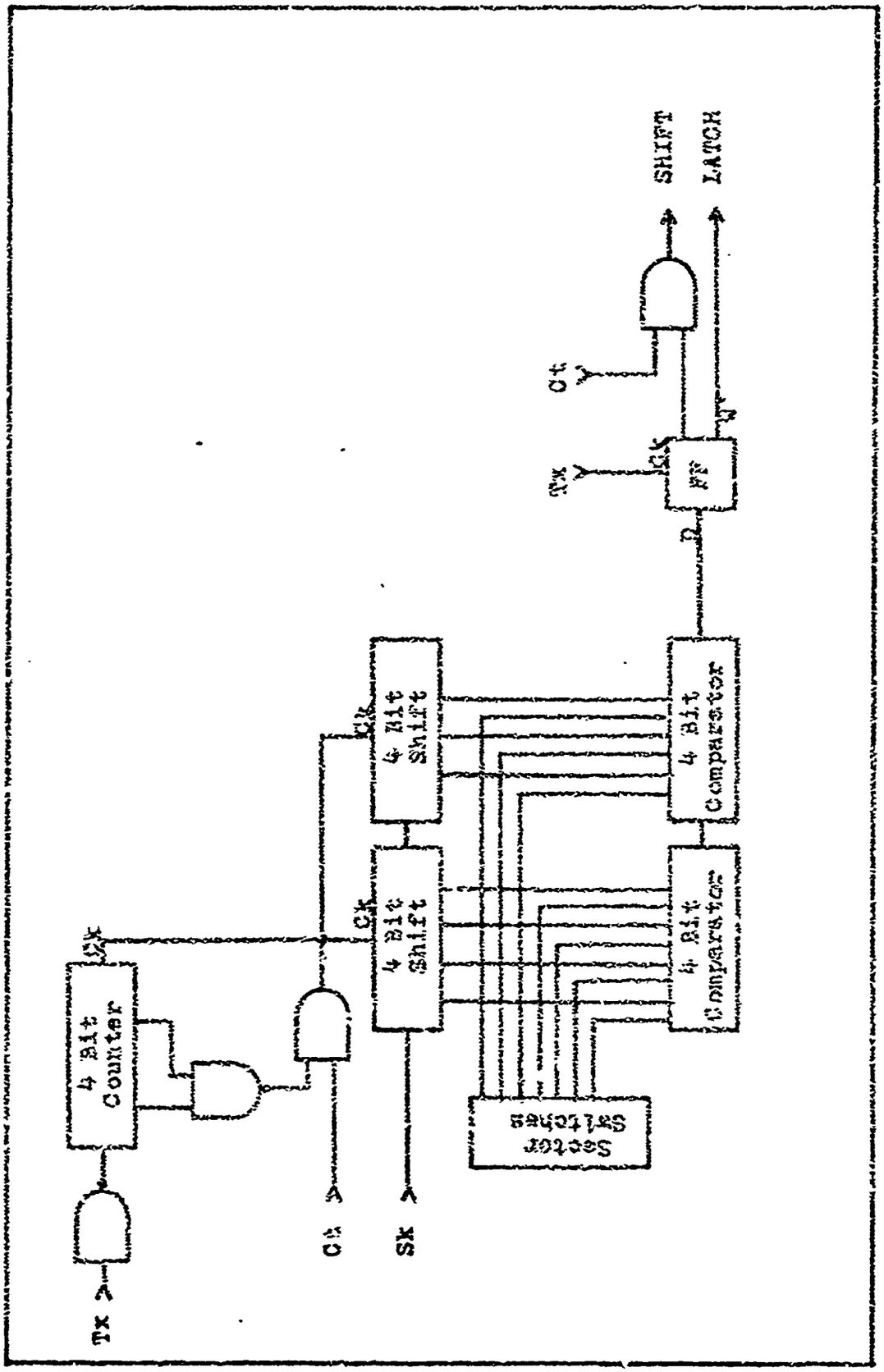


Figure 20. Register Display Circuits (part 1 of 2)

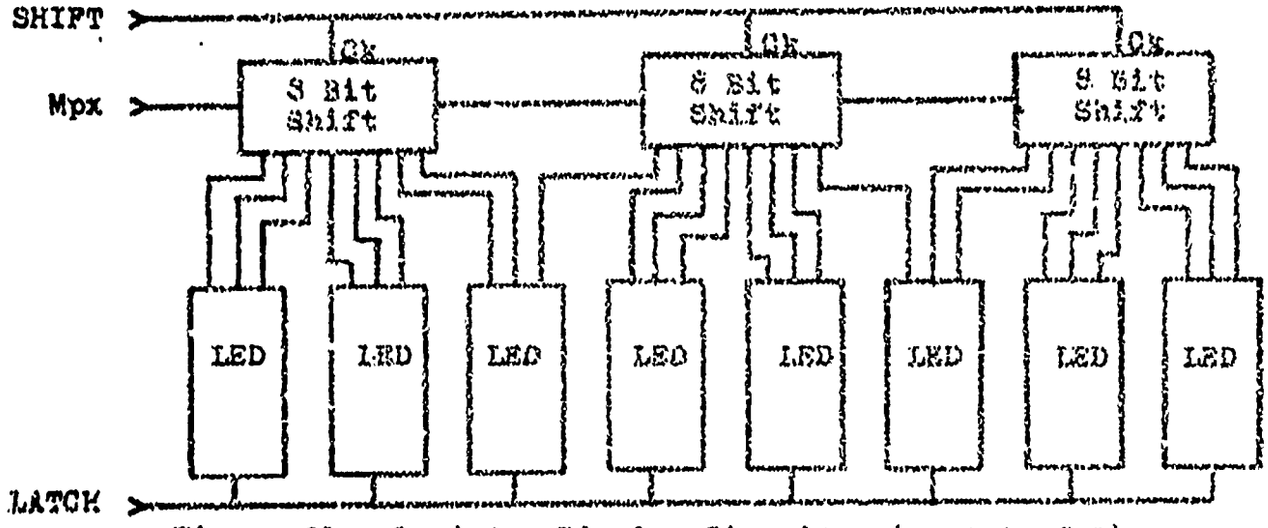


Figure 21. Register Display Circuit. (part 2 of 2)

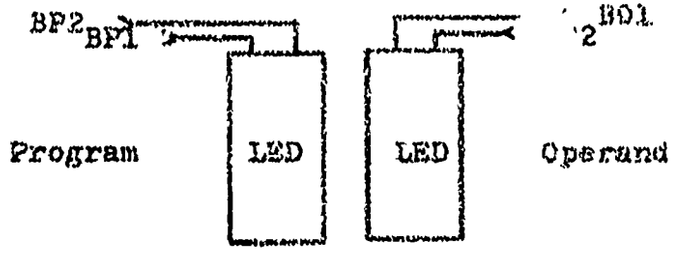


Figure 22. Bank Monitor.

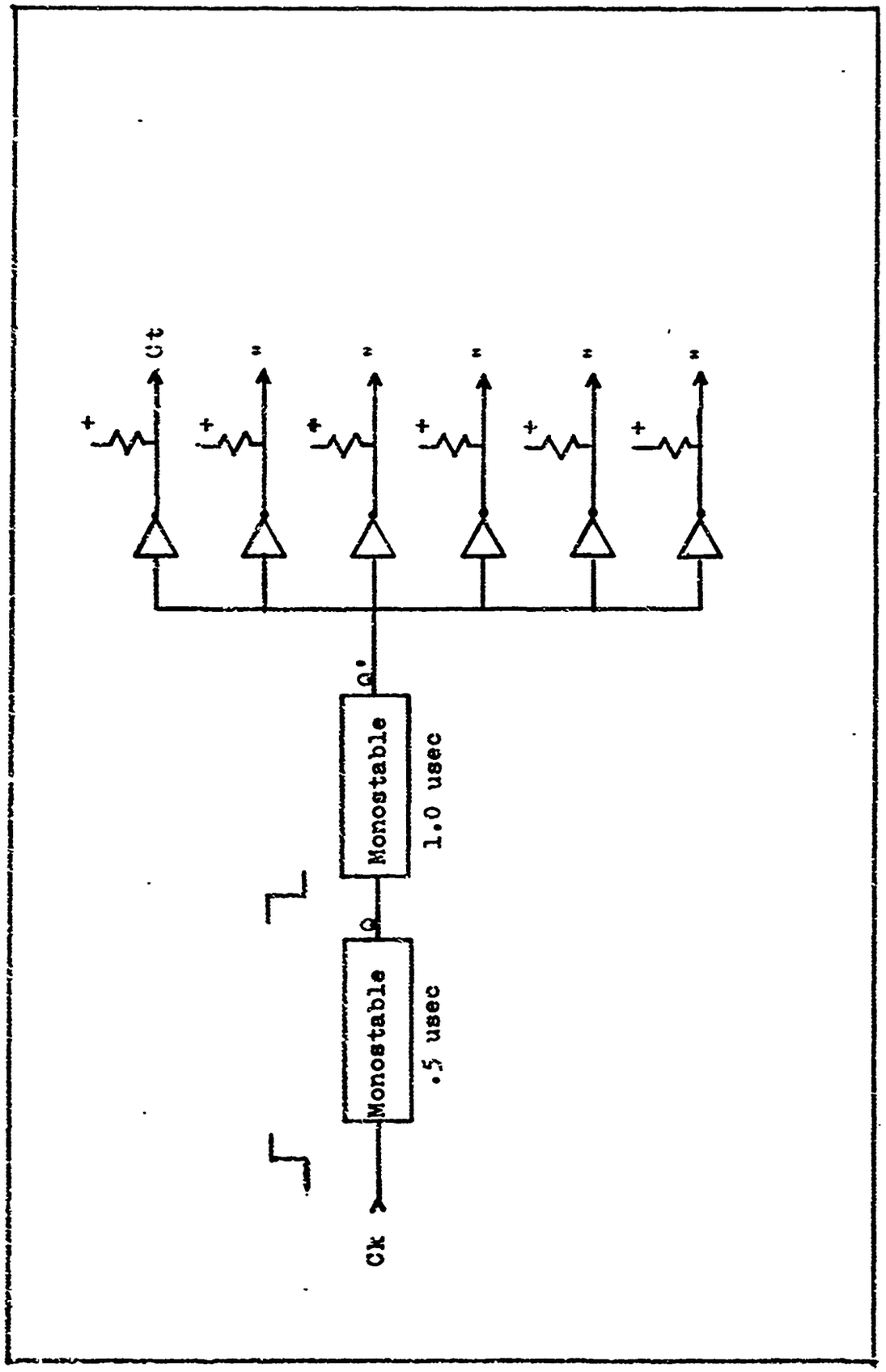


Figure 23. System Clock.

multivibrator provides the .5 microseconds delay and the second provides the one microsecond clock duration. The open collector drivers enable the clock to drive 180 inputs. The buffering was necessary to allow any future additional systems to use the same system clock without additional gate delays.

Conclusions

By interfacing computer signals and using simple TTL logic the computer's operating mode can be controlled and monitored, programs can be entered, and register contents displayed. The circuits developed in this chapter are a solution to the control and monitor problem which meets the requirements of AFIT's application. Others, either more or less complex, may be devised according to the need. Because of similarities in the D37C and D17B the circuits described in this chapter are directly compatible to both, assuming all signals are properly interfaced.

At this point in the process of converting the D37C for general use, these systems, alone, may provide enough control and versatility for many applications. For those which require more, the following chapter presents a method for expansion of D37C I/O capabilities.

IV. Input/Output Expansion

This chapter develops a design to expand the D37C's Input/Output (I/O) capabilities, thereby making it more versatile and compatible with common computer peripherals. Most general purpose applications require computer communications with devices such as teletype writers, tape readers, tape punches, and more. Hence, it is desirable to have such communication capabilities for the D37C so it may be used for general applications. The expanded I/O system is combined with the previously mentioned systems to produce the total converted D37C system shown in the block diagram of Fig. 24.

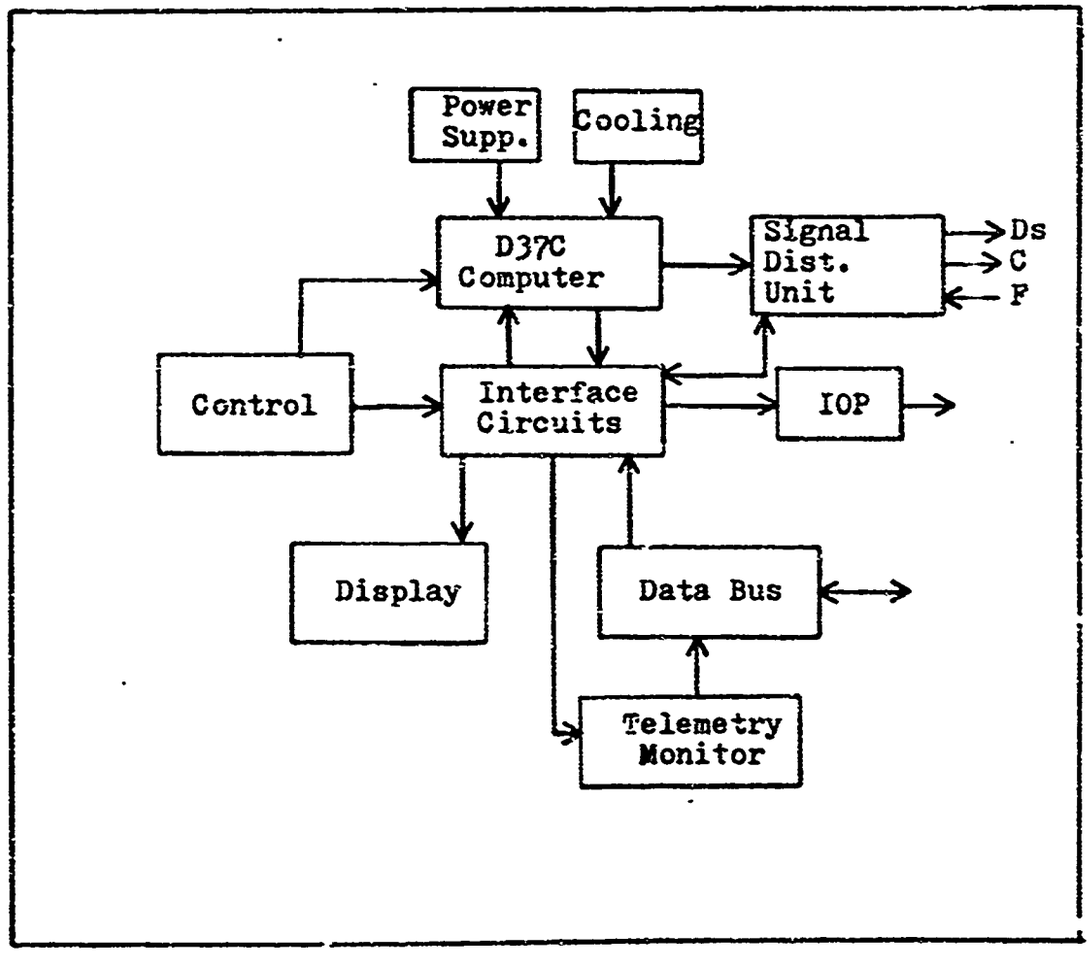


Figure 24. Total D37C System.

Specifications

There are three main design criteria chosen to make the D37C's I/O system more versatile and compatible. They are: developing a program controlled I/O scheme, designing a parallel data-bus structure, and increasing the I/O speed. The feasibility of including Programmed Interrupt, PI, and Direct Memory Access, DMA, facilities is discussed later. The new I/O system should be compatible with the Minuteman systems at AFIT to allow computer-computer communication for possible multi-processor configuration.

Programmed I/O. As the Minuteman operating and software systems develop, it becomes necessary to remove the human operator from the I/O operations. Most general purpose computer applications require many I/O operations and if manual intervention is required the entire operation will be slow and prone to errors. To overcome this, it is necessary to develop computer, or program controlled peripherals and I/O operations. A programmed I/O system should control inputting and outputting information based on the devices' readiness. It should also provide necessary levels and pulses for controlling all peripherals.

Parallel Data Bus. The data path utilized for the programmed I/O scheme may be serial or parallel. A serial method would require very little hardware since a one line bus is all that is needed. However, because at least one instruction (one word time) is needed to input a single bit, serial operation would be very slow (assuming one bit transferred per

disk revolution, about four words per second). A parallel I/O bus requires more hardware but enables many bits of the word (up to 24) to be transferred in a single operation. This is not only faster but better suited for parallel bit peripherals such as tape reader and punch. I/O operations may be made faster by combining a controller with the peripherals to pack information into a full 24 bit word which is transferred in a single operation. Developing the I/O data path as a bus enables peripherals to be added with little or no modifications of I/O expansion circuitry. Paralleling all 24 bit lines will allow the addition of a controller and special equipment such as a graphics display (Ref 12). A full word bus will also aid communications between computers for multi-processing.

Speed Increase. The speed increase of serial operation over parallel, and computer controlled I/O over manual, have already been discussed. There is, however, a further increase in the I/O rate by using a programmed and parallel scheme over the character input program loading mentioned in Chapter III. The computer can receive up to 800 character commands per second. Because it takes nine commands to enter a word into memory, this rate just misses being capable of loading one word per disk revolution, or 100 words per second (11.25 msec to enter 9 commands vs. 10.1 msec for the disk to rotate 129 sector locations). Hence, the character inputs are only capable of 50 words per second for loading consecutive memory locations. A programmed loading scheme can easily transfer one or more words per disk revolution (100 words per second or

more) which makes it much faster than the Character Inputs for loading memory. As software for the Minuteman systems develop, a faster I/O rate will become more important for loading program sections and data blocks.

Organization

Organizing an I/O scheme requires the development of two interdependent subjects, hardware resources and software conventions.

Hardware Resources. The organization of hardware will follow the parallel I/O proposal conceived by Capt. Douglas Allen (Ref 1) and implemented by Lt. Joseph Theriault (Ref 15) for the D17B. The proposal suggests using the only available parallel input port to the machine, the Discrete Inputs. The Discrete Inputs (and Discrete Outputs) are utilized in the missile environment to check and perform a variety of functions (see Appendix A and Ref 3). There are three sets of Discrete Inputs for the D37C, labelled A, B, and C. Set B is the only one capable of loading a parallel 24 bit word and will be used as the programmed I/O input port. Part of the A set will be used to input flags. There are also output signals called Discrete Outputs but cannot be used to output a parallel word since only one from each group may be true at any one time. However, these outputs may be used for other functions such as device select and control lines. An output scheme adapted from work by Joseph Theriault (Ref 15) will utilize a serial port called Telemetry Monitor. This port requires a serial to parallel convertor to produce a parallel word for the data bus.

There is one additional output line that will be utilized to supply a program controlled output pulse. This line is the platform power enable signal and will henceforth be designated the I/O Pulse (IOP). The IOP will be combined with the discrete output lines to generate pulsed control signals.

Software Conventions. Before designing the necessary hardware for an I/O expansion system, one must first have some idea how I/O operations are to be programmed. In an effort to produce the fastest I/C transfers possible the program model should be as short as possible (in word times). There are two basic alternatives for outputting a word as shown in Fig. 25A and B. One is to put the word on the bus and then check the device ready status (flag) before resetting the system and proceeding. Another is to do the flag checking first, then the output operation. Input operations logically follow the model in Fig. 25C, since the flag is the only indication that proper information is on the data bus. Sample code for these three operations is listed in Table V.

A few of the instructions in the model programs need explanation. The store telemetry instruction, XXX/T, may be combined with other instructions and executed in the same word time. In A, it can be combined with instruction number one and thus eliminates one word time of the routine. In B, however, it cannot be combined with number five because output would occur before the data is in the accumulator; and it cannot be combined with seven because the IOP would be generated before the information is on the bus (the IOP signals the de-

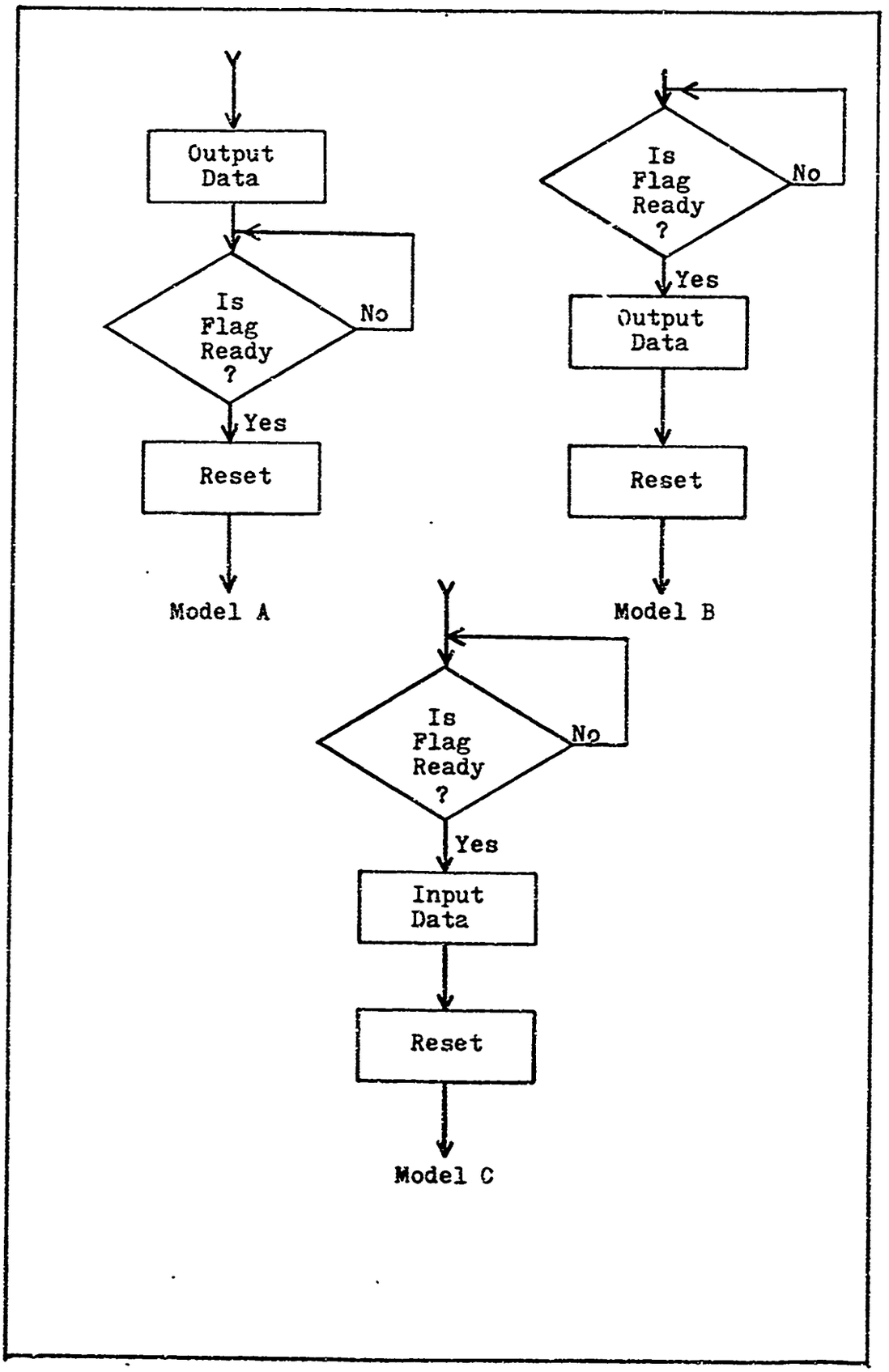


Figure 25. Model I/O Flowcharts.

Table V.

Model I/O Program Blocks

Model	Instruction	Description
Output A		(Data is in Accumulator)
	1. DOAn	Select device to receive data
	2. XXX/T	Output Ac to data bus
	3. GBP	Generate mask to input flag
	4. DIA 1	Input flag
	5. TSZ 3	Transfer on zero to 3
	6. EPP/DPP	Generate IOP
	7. DOA 0	Deselect the device
Output B	1. DOA n	Select device to receive data
	2. GBP	Generate mask to input flag
	3. DIA 1	Input flag
	4. TSZ 2	Transfer on zero to 2
	5. CLA D	Clear and add data to Ac
	6. XXX/T	Output Ac to data bus
	7. EPP/DPP	Generate IOP
	8. DOA 0	Deselect device
Input C	1. DOA m	Select device to produce data
	2. GBP	Generate mask to input flag
	3. DIA 1	Input flag
	4. TSZ 2	Transfer on zero to 2
	5. CLA 6	Clear and add mask to Ac for inputting data
	6. 77777777	Mask (all binary ones)
	7. DIB	Input data word
	8. EPP/DPP	Generate IOP
	9. DOA 0	Deselect the device (data is then stored into memory)

vice to retrieve data from the bus). The Generate Bit Pattern instruction, GBP, and the need to load a mask before data input, results because the Discrete Inputs are ANDed to the Accumulator. Finally, the IOP instruction is a combined instruction of Enable Platform Power and Disable Platform Power.

The rate of I/O transfers is a function of the model program length and how the routines are utilized. If a block of data is to be transferred to/from a single device, the device select and deselect portions are needed only for the first and last transfer. Doing this leaves a four-word-time-routine for Output A, six word times for Output B, and seven word times for Input C. Note, however, that if the flag is not ready when first checked that it will take one disk revolution (10 msec) to check it again. This delay can be minimized by loading the routines in rapid access loops (see Appendix A and Ref 2 and 3). Still, since each word must be retrieved (Output) or stored (Input) into memory after it is transferred, the maximum practical I/O rate is one (or at most two) word per revolution, or 100 words per second.

Design

The design can be divided into three main categories. They are input, output, and control signals.

Input. The input signals required for the I/O expansion system include a 24 bit data word and five general flag signals. The data word is incorporated in a data bus used for both input and output and is also common to all peripherals. This bus structure simplifies the addition of peripherals and

total system design. The data bus terminates as the B Discrete Inputs of the computer. The only hardware logic needed to input the data bus information is the interfacing required to make the two logic types compatible (see Chapter III).

The five flag signals are also developed in a bus structure similar to the data bus. Although only one flag was utilized in the model software it is reasonable to assume that others may be needed to check peripheral status. Four additional flag buses are, therefore, implemented. The flags are terminated as the computer's A Discrete Inputs. As with the data bus, these signals only need interfacing.

Output. The output design requires switching the telemetry output, in parallel fashion, onto the data bus and then removing it at the proper time. The telemetry output, Axt, displays the contents of the Accumulator when a properly flagged instruction is executed. A timing signal, Ptt, indicates when the information is available at Axt. The timing diagram in Fig. 26 illustrates their graphical relationship. It is necessary to use these two signals: first, to shift Axt into a register for serial to parallel conversion; then, to switch this information onto the bus. The IOP is an indication to the peripheral that information is on the data bus and should be latched or stored. After the peripheral receives the data, its flag should be reset until it is ready for more. To give the peripherals time to latch the bus information, the bus will not be cleared until approximately 150 microseconds (about two word times) after the IOP is issued.

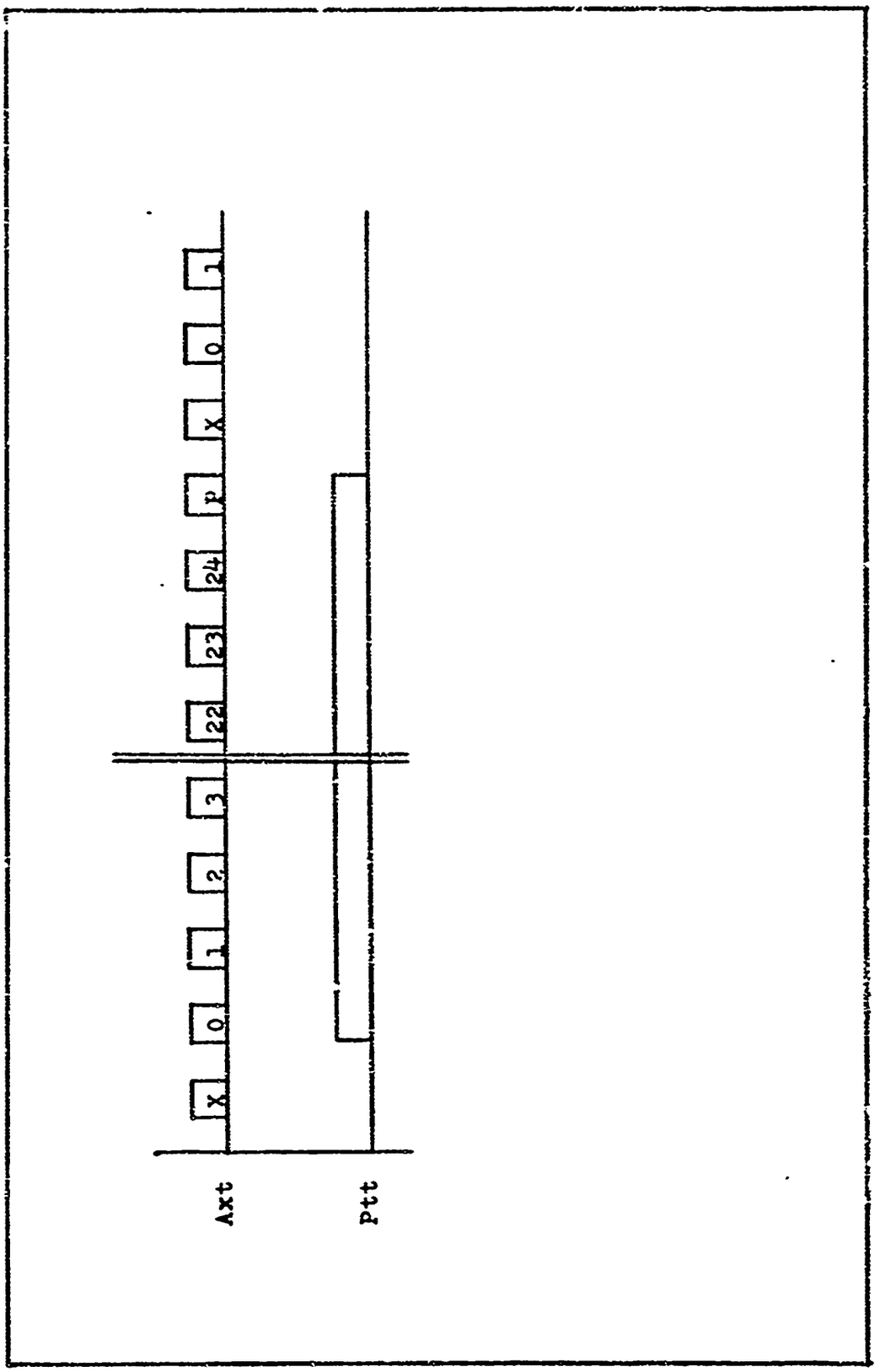


Figure 26. Telemetry Monitor Timing.

Control. The remainder of the output signals are for control purposes. They consist of Discrete Output signals and the IOP signal. There are two groups of Discrete Output signals and both are used for control. The first set, group A, consists of 32 signals and will be designated as Device Select lines, 0 through 31 (DS_n; n=0,1,...31). These lines are enabled individually by an instruction and only one may be true at a time. Each of the DS_n lines may be assigned a peripheral to indicate when a transfer with that device should occur. The DS0 signal is not assigned to a peripheral because becomes true to deselect all the other lines (see Table V). The other group of Discrete Outputs, group B, consists of 15 signals and are designated as Control lines, 1 through 15 (Cm; m=1,2,...15). The control lines are enabled like group A, but they are used for extra control of peripheral functions. Both the Device Select and Control lines may be used for other purposes if the need arises.

The IOP is generated by an instruction and appears on the output labelled E00. The combined instruction of Enable Platform Power (EPP) and Disable Platform Power (DPP) when executed, causes the E00 line to become false for bit times T3 - T5 (Ref 11). Hence, to convert it to the IOP the line needs only to be inverted and interfaced. It is also buffered to drive many loads since it is expected that future users will gate the IOP with Control lines to produce a variety of control pulses.

Realization

To maintain some consistency, the realization will also

be divided into three main areas of input, output, and control signals.

Input. As mentioned, the 24 bit data word port and five flags are implemented in a bus structure. This is done by using gates with open collector outputs to wire AND the functions onto the bus. Negative logic is used on the bus so the AND function becomes a wired OR. In this way, the data bus may be used for both input and output operations, and allows peripherals to be added on the bus without affecting others.

Fig. 27 shows a typical circuit used for both data and flag inputs. The 1K resistor is the common collector, or pull up resistor required by the open collector outputs on the bus. The invertor converts the bus to positive logic before being interfaced by the inverting line driver. The line driver converts the TTL logic signal to a signal compatible with computer input requirements (Ref 5). If non-inverting line drivers

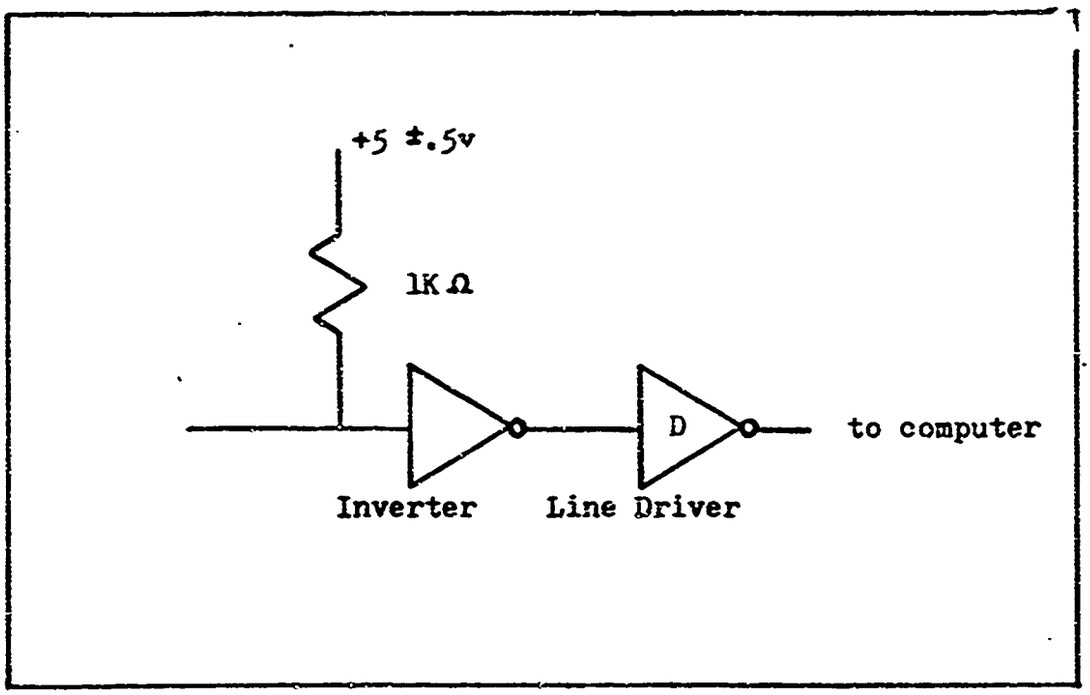


Figure 27. Example of Data Bus and Flag Bus Input.

or some other type of non-inverting interfacing is used, the inverters may be eliminated.

The first five linss of the data bus, D1 - D5, are combined with the character inputs, I1 - I5, mentioned in Chapter III. Doing this allows the same bus to be used for memory loading in both compute and non-compute states.

Output. The computer output information must first be converted from serial to parallel, then gated onto the data bus. This is done by shifting Axt into a 24 bit shift register as shown in Fig. 28. The Axt information is delayed one bit time which allows Ptt to be used directly to gate the shift pulses (see Fig. 26). The information in the register is switched onto the data bus by 24 open collector output NAND gates. The switch signal is controlled by Ptt' and the IOP. The Ptt' signal clears the flip-flop and switches the register onto the bus. For one word time, the data will be changing as the word is shifted into the register and should not be latched by the peripheral. The IOP signals when to latch the data and must occur after the shift. The switch signal remains true until approximately 150 microseconds after the IOP. The negative going edge of the IOP triggers the monostable which in turn clocks the flip-flop. The negative edge of the monostable pulse clocks the output to a fal- hich removes the data from the bus. The two open collector inverters are needed to drive the 24 gate inputs.

Control. The remaining circuits include Device Select, Control and IOP signals. All of these signals are interfaced

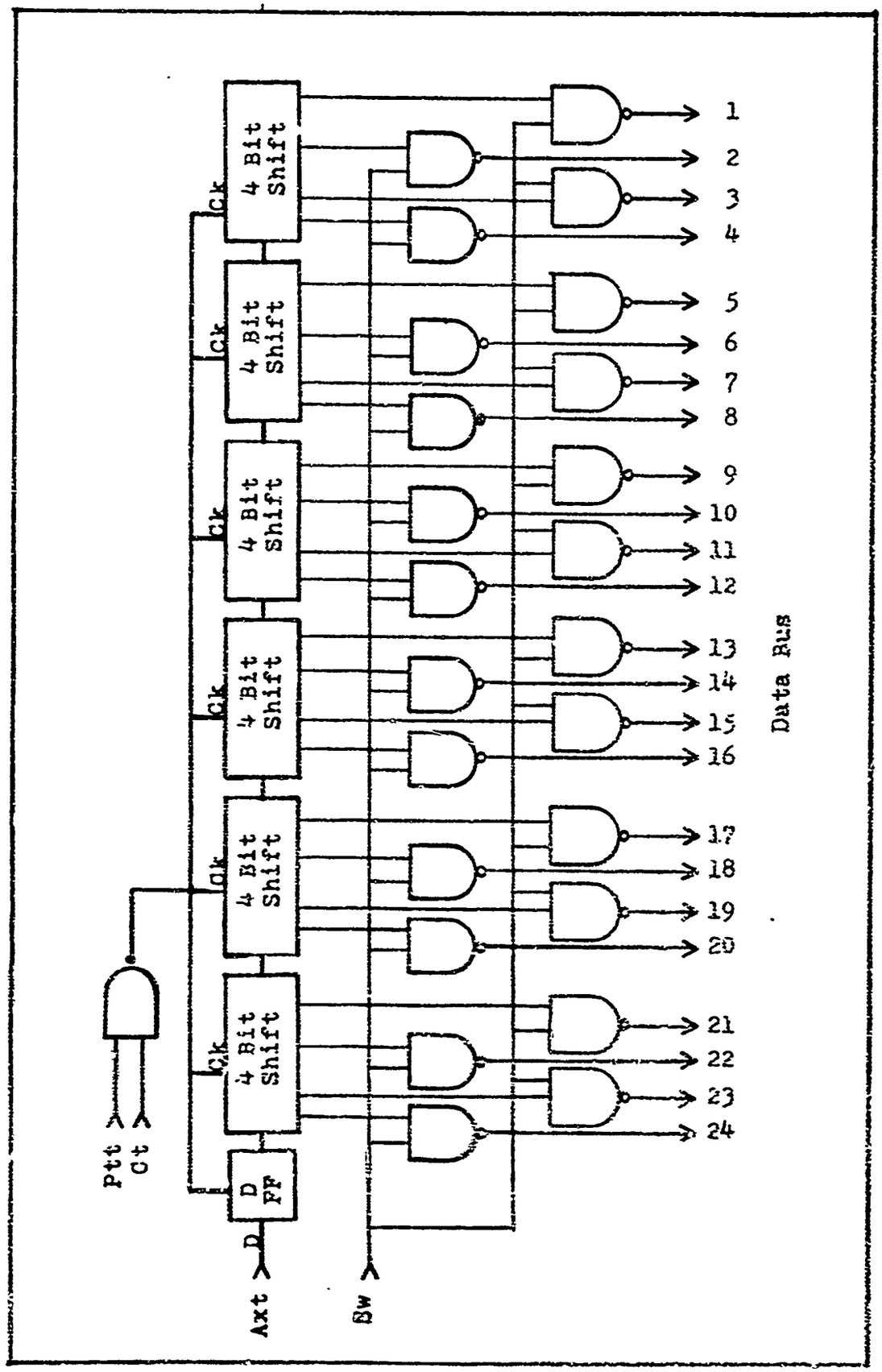


Figure 28. Output Schematic. (page 1 of 2)

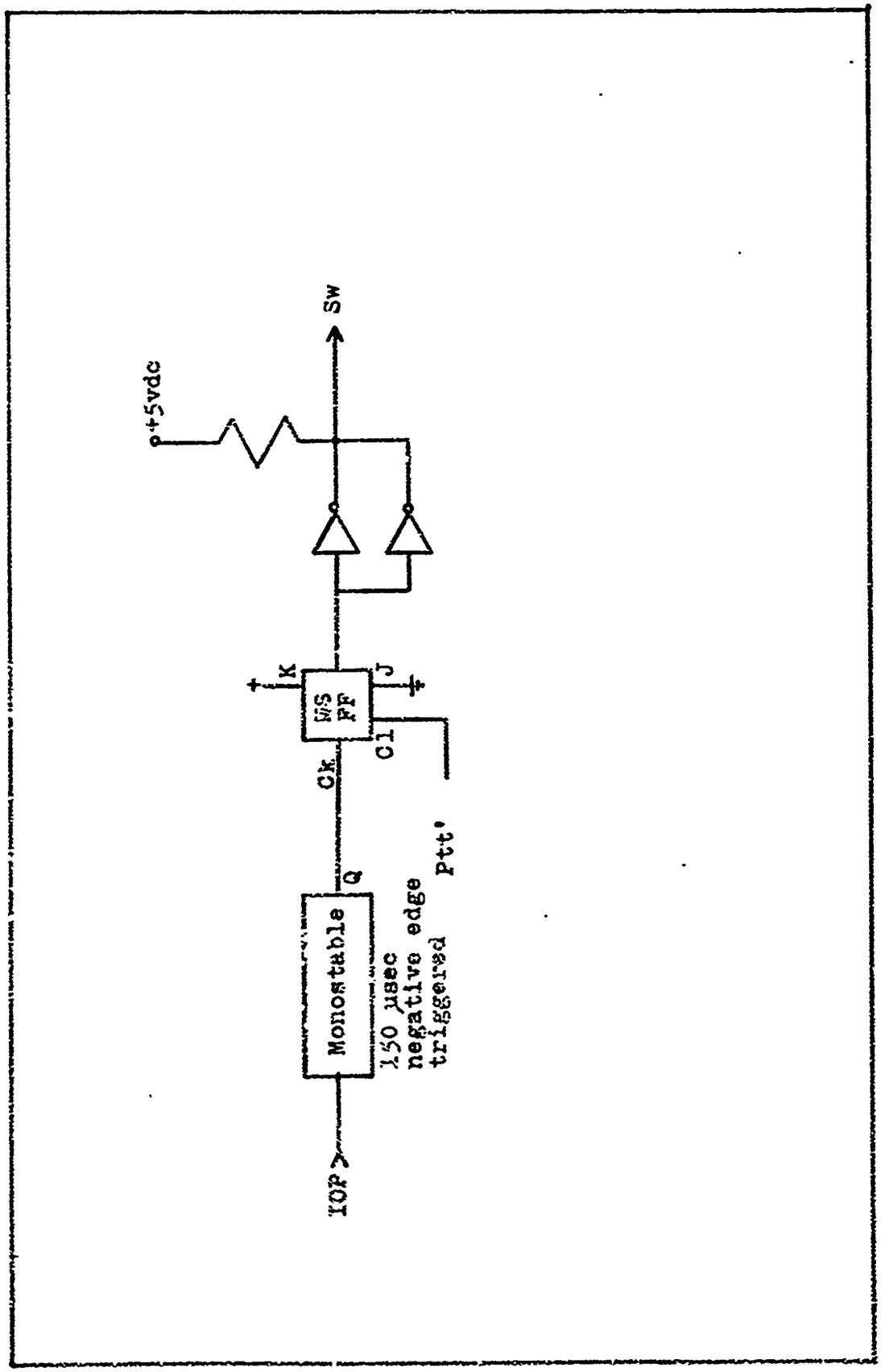


Figure 28. Programmed Output Schematic. (page 2 of 2)

with line receivers and terminated at the Signal Distribution Unit (SDU). The SDU is located on top of the console and allows easy access to all control signals. The location of SDU signals is shown in Fig. 29. The IOP will be used in many circuits and is therefore buffered to accomodate up to 60 gate inputs. The schematics for the IOP and other control signals may be found in Appendices B and C.

Peripheral Interface Specifications

To interface peripherals to the D37C's expanded I/O system, certain conventions and requirements must be met. These may be categorized as hardware or software requirements.

Hardware. Any peripheral connected to the I/O system must be interfaced in a way shich won't interfere with other peripherals or I/O operations. Connections to the data bus must be made with open collector TTL gates. Negative logic shall be used to obtain the proper sense when information is transferred. At least one Device Select line shall be dedicated to each peripheral and used to gate information onto the data and flag buses. In addition, output information should not be latched before the IOP or later than 150 microseconds after the IOP. If these hardware restrictions are met, peripherals shall be capable of communicating with the computer, providing certain software conventions are also met,

Software. I/O software for this system must follow one of the three models mentioned previously plus meet a few additional requirements. At initial start up the switch flip-flop (see Fig. 28) in the output circuit will be in a random

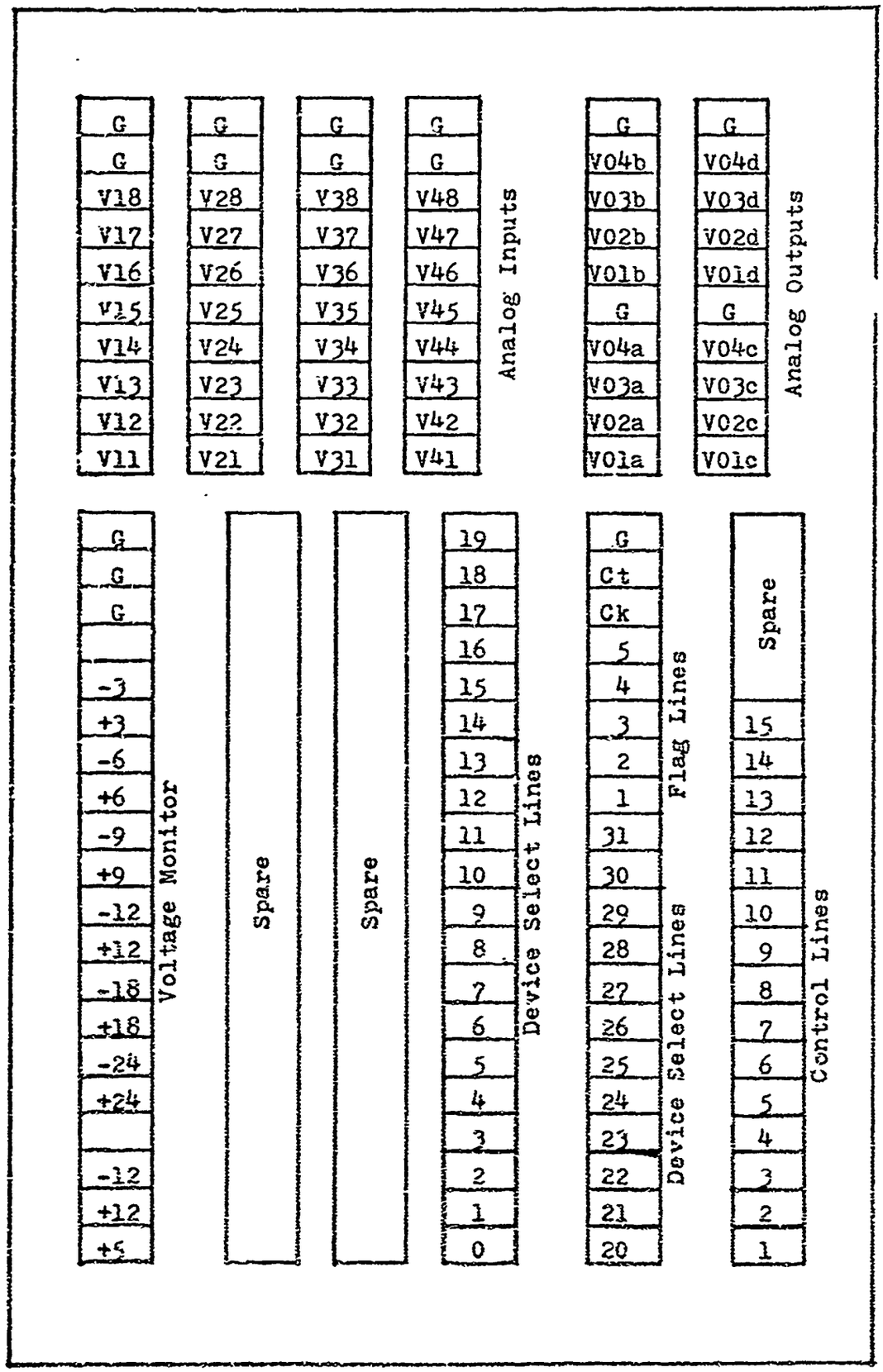


Figure 29. Signal Distribution Unit.

state which may switch erroneous data onto the bus. Therefore, the output switch flip-flop must be reset after initial start up by issuing an IOP at least two word times before the first I/O transaction. Peripherals and flags for peripherals must be preset according to their specification before the initial transfer. This is also done with an IOP that is gated with Control Signals. The programmer must insure a mask is present in the accumulator before data or flags are transferred (this is different from the D17B system which needs no masks (Ref 15)). The IOP shall not be generated within one word time after a telemetry store instruction. This is to allow the information to be shifted into the output register. Finally, because of the IOP delay in the output circuit, consecutive output operations should be spaced at least three word times. This last restriction should present no problem since flag checking provides ample spacing.

Conclusion

This chapter illustrates that a few simple circuits can convert the specialized I/O system of the D37C computer into one more versatile and compatible with most minicomputer peripherals. The system developed provides programmed controlled I/O capabilities, a parallel port for both input and output, and increased speed for memory loading. It also produces a very versatile and nonrestrictive system. The data bus may be shorter (say 8 bits), at first, and then expanded to a full parallel word when a controller or some other device makes it necessary. The Device Select and Control lines have not been

dedicated to any special purpose and may have many functions. Several undedicated flags are also available for checking peripherals status. The final I/O system shall make the D37C more useful in applications requiring more versatile communications between computer and external devices.

Additional I/O features, such as Direct Memory Access (DMA), and Program Interrupt (PI), were investigated for inclusion into the D37C I/O system. These features, however, required hardware modifications of the computer which fell outside the scope of this report. Lt. Joseph Theriault designed a DMA output facility for the D17B by using the Mpx output (Ref 15) and Capt. Duane Reynolds designed a D17B, DMA input facility through hardware modifications (Ref 13). However, because the D37C's Mpx output cannot randomly display the memory, a similar DMA could not be designed (Ref 5). A similar PI facility to that designed by Lt Theriault (Ref 15) could not be designed because of no external indication of the program channel. However, flag polling could be programmed for the D37C system as a substitute, if such a feature is desired. The absence of both the DMA and PI facilities should not be a severe handicap for the D37C system since these features are not important in many applications.

V. Summary

This chapter consists of a final system description, a summary of conclusions, and a few suggestions for future research topics.

Final System Description

To convert the D37C for general purpose applications and to fulfill the objectives of this investigation, the three systems developed in this report are combined to produce the final system. The D37C conversion system is an interconnection of the Power and Cooling, Control and Monitor, and I/O Expansion subsystems.

Interconnections. The subsystems are connected by various plugs and cables which run throughout the console. Power for all circuits and the computer is routed through the Power Distribution Unit (PDU) which supplies fusing for all power and provides a central location for power troubleshooting. It will also provide +5vdc current (up to 3.5 amps) for future systems placed in the console.

Other signals to and from the computer housing are routed through two circuit boards, one for outputs (I1) and one for inputs (I2). A few signals, such as voltage monitor and analog signals, are routed from the computer directly to the Signal Distribution Unit (SDU). The computer signal cables are fabricated from stranded wire to avoid breaking due to bending. A few computer outputs, such as the clock and sector signals, are designed to drive a shielded cable and are therefore con-

nected to the interface boards with 75Ω coax. Shielded cable is not used elsewhere because of possible signal degradation from mismatched lines and twisted pair was not used due to the absence of complement signal sources. Signal routing between the console circuit boards is done with 16 and 14 lead stranded flat cable. This cable was selected because it is easily connected to boards by using IC sockets, and the cables are easily fabricated. A complete listing of all console and computer signals and associated cabling is given in Appendices B and C.

Physical Locations. The major components of the computer console may be located in Fig. 30. The bottom shelf contains the PDU and power supplies (+5, +12, -12vdc) for the circuits. The second shelf supports the computer, circulating pump, and cooling fans. Both shelves slide out for easy access. The SDU is located on top of the console under a hinged access door. The SDU supplies easy access to analog input and output, voltage monitor, Device Select, Control, and Flag signals.

The console front panel is illustrated in Fig. 31. The cooling, console, and computer power switches are located in the lower left hand corner. The middle of the panel contains the mode control switches and mode indicators. On the right side, the program load keyboard is near the bottom, the display select thumbwheels are in the middle, and the register display is on top. If a simple I/O device is needed, there is room remaining along the top of the front panel for a 24 bit switch and display register similar to the one on the D17B I/O

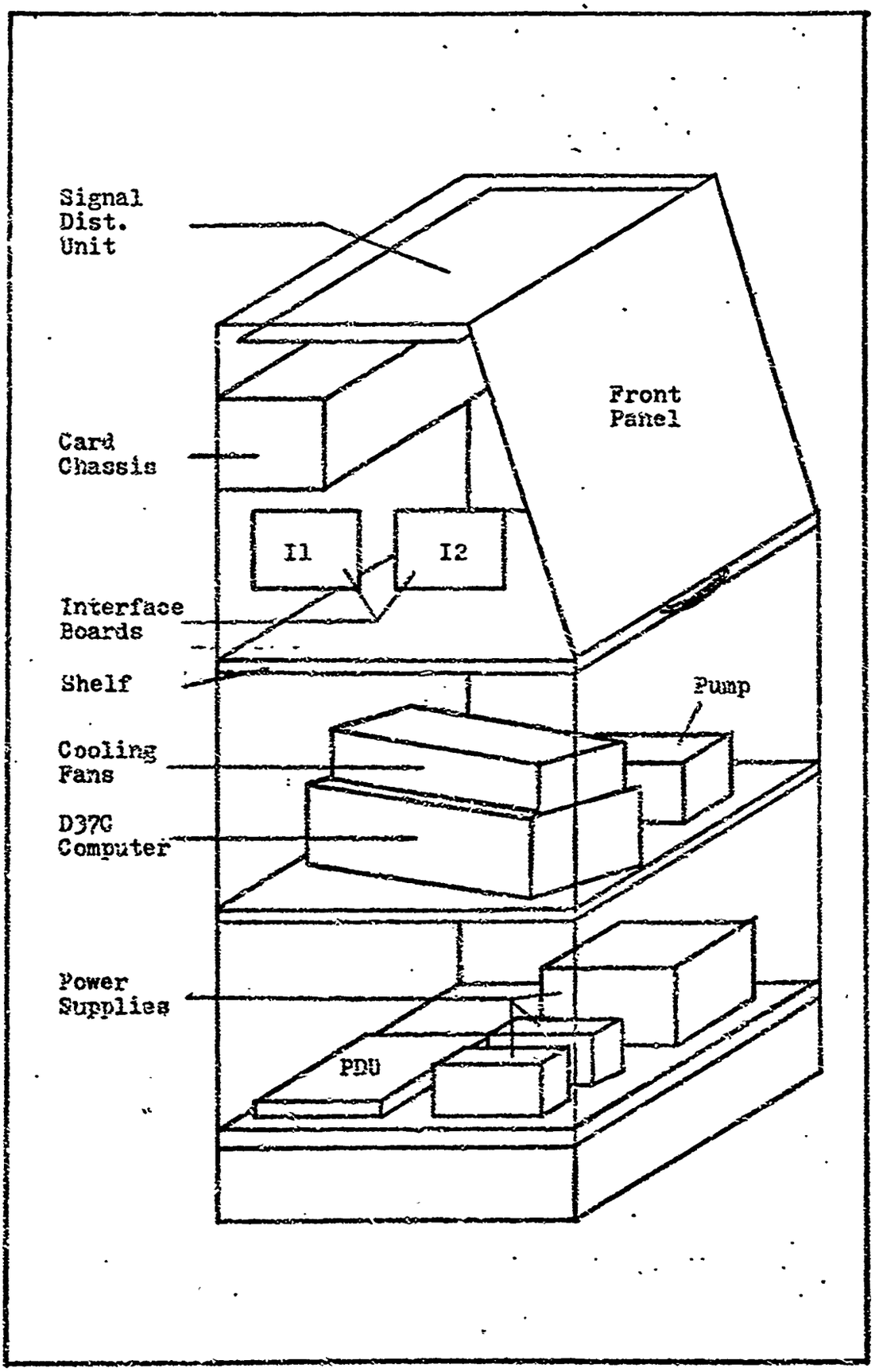


Figure 30. System's Physical Locations.

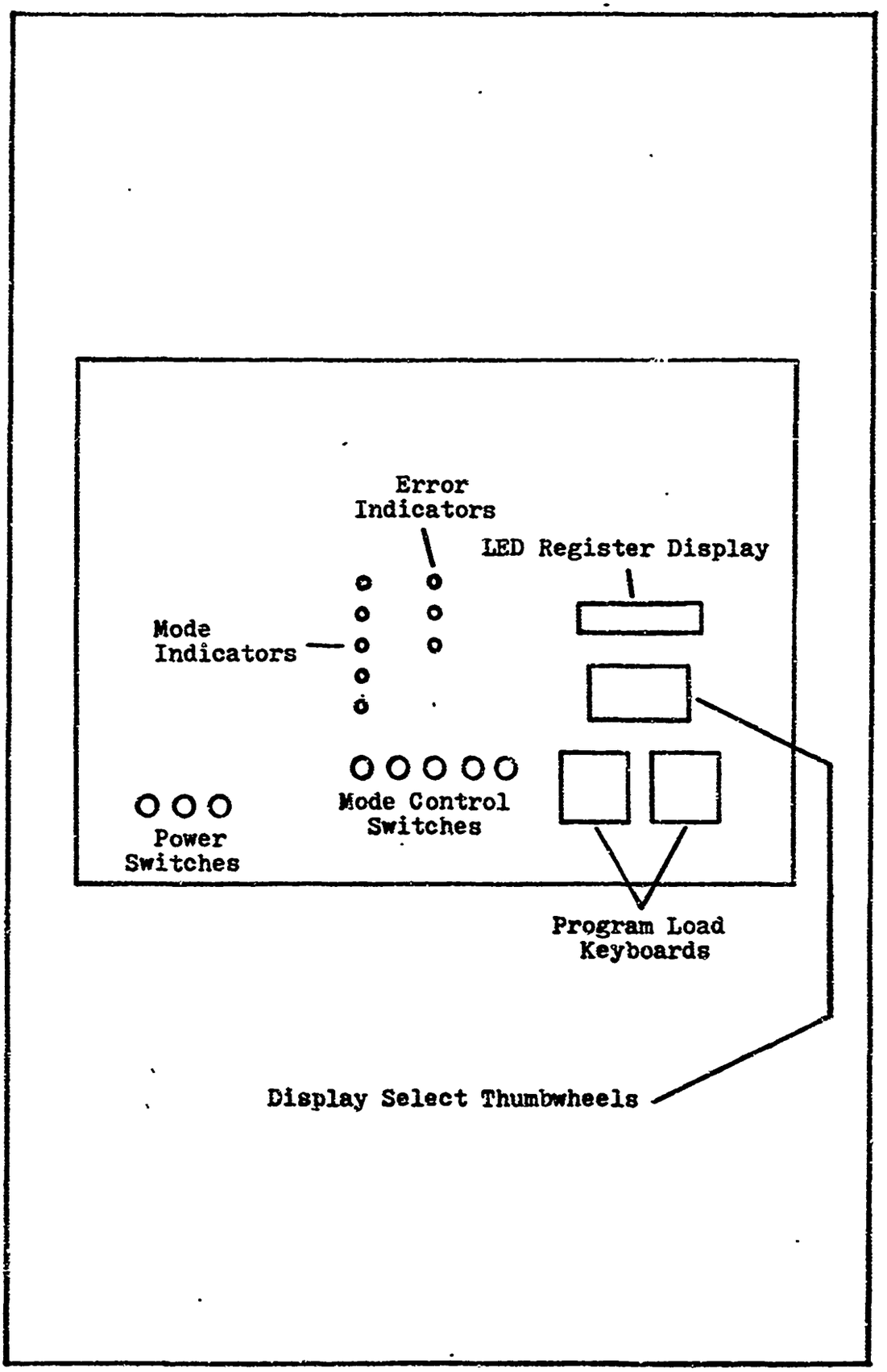


Figure 31. Console Front Panel.

console at AFIT (Ref 7).

All of the circuits for the console are located on four circuit boards. The interface boards, I1 for outputs and I2 for inputs, are located on the side of the console in close proximity to both computer and other circuits. The panel circuit board, PB, is mounted on the back of the front panel and contains the Register Display, Bank Indicator, Program Load, and Mode Control circuits. The final board, A, and future peripheral interface cards are located in the card chassis. Board A contains the I/O Output , Mode Display, System Clock, Channel Select, and IOP Driver circuits. Additional future systems should be located in the card chassis filling in locations from right (A is rightmost) to left.

Conclusions

Chapters II, III, and IV of this investigation developed systems to convert the D37C Minuteman computer for general applications. The systems include Power and Cooling, Control and Monitor, and I/O Expansion.

Power and Cooling. Strict specifications were given for power and cooling systems development. Noting that these restrictions were intended to simulate a missile environment they were relaxed in order to utilize available equipment. The resulting cooling and power systems are simple and easily fabricated.

Control and Monitor. The systems necessary to control and monitor computer modes and transitions,resulted in some very simple circuits. The systems were expanded slightly to

include a simple I/O scheme called program load and register display. The scheme shall prove invaluable in debugging programs and may be sufficient I/O for many applications.

I/O Expansion. For applications requiring more versatile and compatible I/O the expanded system was developed. The Expanded I/O system provides program control, a parallel I/O port, and increased speed. By utilizing many of the available signals from the computer, the system circuits are relatively simple. The program models and peripheral interface conventions provide a basis for a highly versatile I/O system.

Recommendations

The following recommendations are suggested to expand the D37C's usefulness as a general purpose computer and educational machine.

1. Peripherals Interfaced - Peripheral devices may be added to the system to provide auxilary storage and expanded man-machine communications. Devices such as a teletypewriter, paper tape reader, and tape punch may be interfaced with simple logic circuits (Ref 10).

2. Software Development - Many programs and subroutines are required before the D37C can be considered a true general purpose machine. Loaders, assembler, and operating system are needed to raise the system above the machine language programming level. The programs may be written for the D37C in a stand alone system or assembled on a larger computer if one is available.

3. Hardware Modifications - Certain modifications to the

machine may be investigated to expand its capabilities. A Direct Memory Access Facility could be developed if modification of the read/write circuitry is feasible (Ref 13). A Program Interrupt capability would be possible if the selected program channel could be monitored internally (Ref 15). Finally, the speed of execution may be increased by raising the memory power frequency (see Chapter II).

4. Console Improvements - There are several possible improvements to the console that would make it more reliable and a better educational tool. Simple power and cooling monitoring circuits could be fabricated to sense external power sources and the computers temperature. If they became out of tolerance the power to the computer could be automatically disconnected, thereby preventing possible damage. Another improvement would include a switch register and bus display for a simple educational peripheral (Ref 15). Finally, a revolution counter may be added as an input device on the bus. It would serve as a real time clock and prove invaluable for timing program segments and developing optimum software (Ref 11).

5. Special I/O Devices - Special I/O devices may be developed for the D37C to aid its practical and educational usefulness. Because the D37C has built-in Analog-to-Digital, and Digital-to-Analog converters, it would be a simple matter to build a peripheral to check IC's. The converters would also be suitable for controlling experiments with analog sensors or controls. Special devices developed in the logic lab at AFIT, such as the Character Display by Capt. Trimble (Ref 18) and

the Graphics Display by Lt. Kennedy (Ref 12) may also be interfaced with the D37C to expand the system's capabilities.

Concluding Statement

The purpose of this study is to investigate the feasibility of converting a Minuteman guidance computer, the D37C, for general purpose application. It has been shown the computer can be set up and operated by fabricating a few simple circuits and systems. If more than minimal I/O capabilities are required, the expanded I/O system may be added to make the machine compatible with a wide range of peripherals. In summary, the machine can be converted to general use for a relatively small investment of time and money. The conversion process may provide Air Force laboratories and/or civilian institutions with highly reliable, low cost computing power when the machines become surplus.

Bibliography

1. Allen, Douglas J. Laboratory Conversion and State Description of the D17B Computer. Wright-Patterson Air Force Base, Ohio: Air Force Institute of Technology, June, 1972. DDC: AD 746 908.

2. Autonetics. D37C Minuteman Computer Logic Breakdown. (Technical Memorandum 64-343-2-8). Anaheim, California: Autonetics, Division of North American Rockwell, Inc.

3. Autonetics. "Minuteman" D37C Digital Computer System Depot Overhaul. Anaheim, California: Autonetics, Division of North American Rockwell, Inc. FET-D-120-D37/4

4. Autonetics. Minuteman Logical Description D37C Computer. (Unpublished Notes). Anaheim, California: Autonetics, Division of North American Rockwell, Inc.

5. Autonetics. Test for Repair and Recycle, Specifications, AA0205-1784. Anaheim, California: Autonetics, Division of North American Rockwell, Inc., 22 May 1967.

6. Beck, Charles H. (ed.) Proceedings of the Fourth Meeting of the Minuteman Computer Users Group, MCUG-4-72. Tulane University, New Orleans, Louisiana, June, 1972.

7. Booth, Taylor L. Digital Networks and Computer Systems. New York: John Wiley and Sons, Inc., 1971.

8. Brady, R. C. and Charlie D. Huskey. Design and Fabrication of a Control Console for the Minuteman D17B Computer. Wright-Patterson Air Force Base, Ohio: Air Force Institute of Technology, March, 1972. DDC: AD742437.

9. Hill, F. J. and G. R. Peterson. Introduction to Switching and Logical Design. New York: John Wiley and Sons, Inc., 1968.

10. Lundy, Richard M. Input-Output Interfaces for the D17B Bus-Structured I/O System. Wright-Patterson Air Force Base, Ohio: Air Force Institute of Technology, June, 1974.

11. Kee, W. T. Programming Manual for the D37C Computer. Anaheim, California: Autonetics, Division of North American Rockwell, Inc., 30 January 1965.

12. Kennedy, Jeri. Design and Synthesis of a Vector-Graphics System. Wright-Patterson Air Force Base, Ohio: Air Force Institute of Technology, March, 1974.

13. Reynolds, Duane B. Design Expansion of the D17B Computer Facility. Wright-Patterson Air Force Base, Ohio: Air Force Institute of Technology, November, 1973.

14. Schaff, Robert M. Development of Input/Output Interface for the D17B Computer. Wright-Patterson Air Force Base, Ohio: Air Force Institute of Technology, March, 1972. DDC: AD 742 438.

15. Theriault, Joseph R. T. Design Expansion of the D17B Computer Input/Output Facility for General Purpose Applications. Wright-Patterson Air Force Base, Ohio: Air Force Institute of Technology, March, 1973. DDC: AD 760 761.

16. Texas Instruments, Inc. Designing with TTL Integrated Circuits. New York, New York: McGraw-Hill Book Company, 1971.

17. Texas Instruments, Inc. The Integrated Circuits Catalog for Design Engineers, CC401. Dallas, Texas: Texas Instruments, Inc., February, 1971.

18. Trimble, Thomas N. A Cathode Ray Tube Display System for a Minuteman I Computer. Wright-Patterson Air Force Base, Ohio: Air Force Institute of Technology, December, 1973.

APPENDIX A

D37C Computer Description

Appendix A

D37C Computer Description

This appendix contains supplemental information about the D37C computer. The computer's functional units are described and programming is discussed.

Functional Computer Unit Descriptions (Ref 3)

Control Unit. The control unit interprets and processes all machine functions and is comprised of a location counter, the instruction register and the phase register.

1. Location Counter - The location counter determines the channel from which the next instruction is to be obtained.

2. Instruction Register - The instruction register holds the instruction to be executed by the computer. This instruction defines the type of operation to be performed such as add, subtract, etc.; specifies the location address of the operand when necessary and indicates the sector address of the next instruction.

3. Phase Register - The phase register consists of three flip-flops which may be set to one of eight possible states to indicate the phase of flight. It also serves as a selector switch to determine which group of voltage inputs are to be sampled and as an index register for a modify-flagged instruction. The state of the phase register is available as the stage reference outputs.

Arithmetic Unit. The arithmetic unit is comprised of

three registers: the accumulator (A), lower accumulator (L) and the number register (N). Only the A and L registers are addressable.

1. Accumulator (A-register) - The accumulator serves as the main register of the computer and holds the results of all arithmetic operations. This register serves as an output register for telemetry and character outputs.

2. Lower Accumulator (L-register) - This register is used for certain arithmetic, input, logical operations or for rapid access storage.

3. Number Register (N-register) - This register is used by the logic of the computer during multiplication and division and is not addressable.

Input Unit.

1. The discrete input lines generally serve as communication lines from external equipment. There are three sets of "on - off" type signals:

a. One set samples 24 input signals.

b. One set samples 19 external input signals and 5 flip-flops from within the computer.

c. One set samples 21 input signals, two flip-flops and the logical "or" of 7 discrete output signals.

2. Program Load - The main input for loading numerical data and instructions into the computer memory is a punched tape (paper or mylar). Information can be entered into the computer at a maximum rate of 800 five-bit codes per second

from a photo-electric tape reader. Data can be entered manually from a keyboard if a computer manual control panel (CMPC) is available.

3. Detector - The detector input is an "on - off" type signal received from an external source and indicates the working status of a specified piece of external equipment. The detector input monitor can be "reset" by means of a special instruction.

4. Incremental - The incremental inputs are basically independent of program control and consist of seven resolver type, two variable incremental type and one pulse type. These inputs are accumulated in the two four-word input buffer loops (V&R).

5. Voltage - The computer is capable of converting one of 32 dc voltage inputs into an 8-bit binary number under program control. Analog voltages are grouped into four sets of eight inputs each. The range is $\pm$ 10 volts with an accuracy of 200 mV.

6. Cable - Cable inputs are serial messages of up to 96 bits in length entered into one of the four words of the C-loop. Maximum data rate in 1600 bits per second. Cable input operation is begun by executing the Enable Cable Input instruction and proceeds basically independent of program control.

7. Radio - Radio inputs are serial messages of unlimited length entered into one word of the C-loop. After 24 bits are accumulated, the information is transferred to chan-

nel MX Sector 054 and the loop is prepared to accept another 24 bits. Maximum input data rate is 100 bits per second. The operation is begun by an instruction and proceeds basically independent of program control.

8. External Reset - Master Reset (Mr), Enable Write (Ew_c), Initiate Load (Fs_c) for checkout only, Halt Prime (K'_{h_c}), Run Prime (K'_{r_c}), Single Cycle Prime (K'_{s_c}).

Output Unit.

1. Discrete - The discrete outputs provide two independent sets of output lines (32 and 15) for a total of 47 "on - off" type signals. The outputs are modified under program control and are sent to equipment external to the computer.

2. Voltage - There are four dc voltage output lines available with each proportional to an 8-bit number including the sign. These lines are updated at the rate of 9.27 volts per 32 word times. The range is $\pm$ 10 volts with an accuracy of $\pm$ 200 mv.

3. Single Character - The single character output provides four-bit characters suitable for typewriter, tape punch or other similar output equipment. A parity check bit and two timing bits are issued automatically with each character.

4. Cable - The cable output is a serial message of up to 96 bits in length transmitted from the four word C-loop. The maximum data rate is 1600 bits per second. The operation is begun by execution of the Enable Cable Output (ECO) instruc-

tion and proceeds basically independent of program control.

5. Binary - There are four pairs of outputs which can be used to control external equipment such as gyro, etc. The output states are automatically updated under program control every 10 MS. The output is in the form of +1 or -1.

6. Telemetry - A timing signal is issued under program control which signifies that the accumulator contains information which is to be read by the external equipment receiving the timing signal.

7. Miscellaneous - These signals include Parity/Verify error signal, mode indication and stage reference.

Memory Unit. The D37C computer memory consists of a rotating magnetic disk driven by a synchronous motor at 6000 rpm. Adjacent to the disk are two fixed head plates which house the read and write heads. The disk has a thin magnetic oxide coating on both sides for storing information. This disk is supported by air bearings generated by the rotating disk. The disk is divided into tracks or channels of 128 words each for main memory. A total capacity of 7222 words may be contained in the 56 channels of 128 Sectors, six 4-word loops, one 8-word loop, one 16-word loop and six 1-word loops.

Programming

The computer uses a full 24 bit instruction word and data word. Data is represented in one of two fashions, as a 23 bit binary fraction (full word) or as a 10 bit fraction (split word). The two formats are shown in Fig. 32. Instructions also have two formats, either flagged or unflagged as indicated

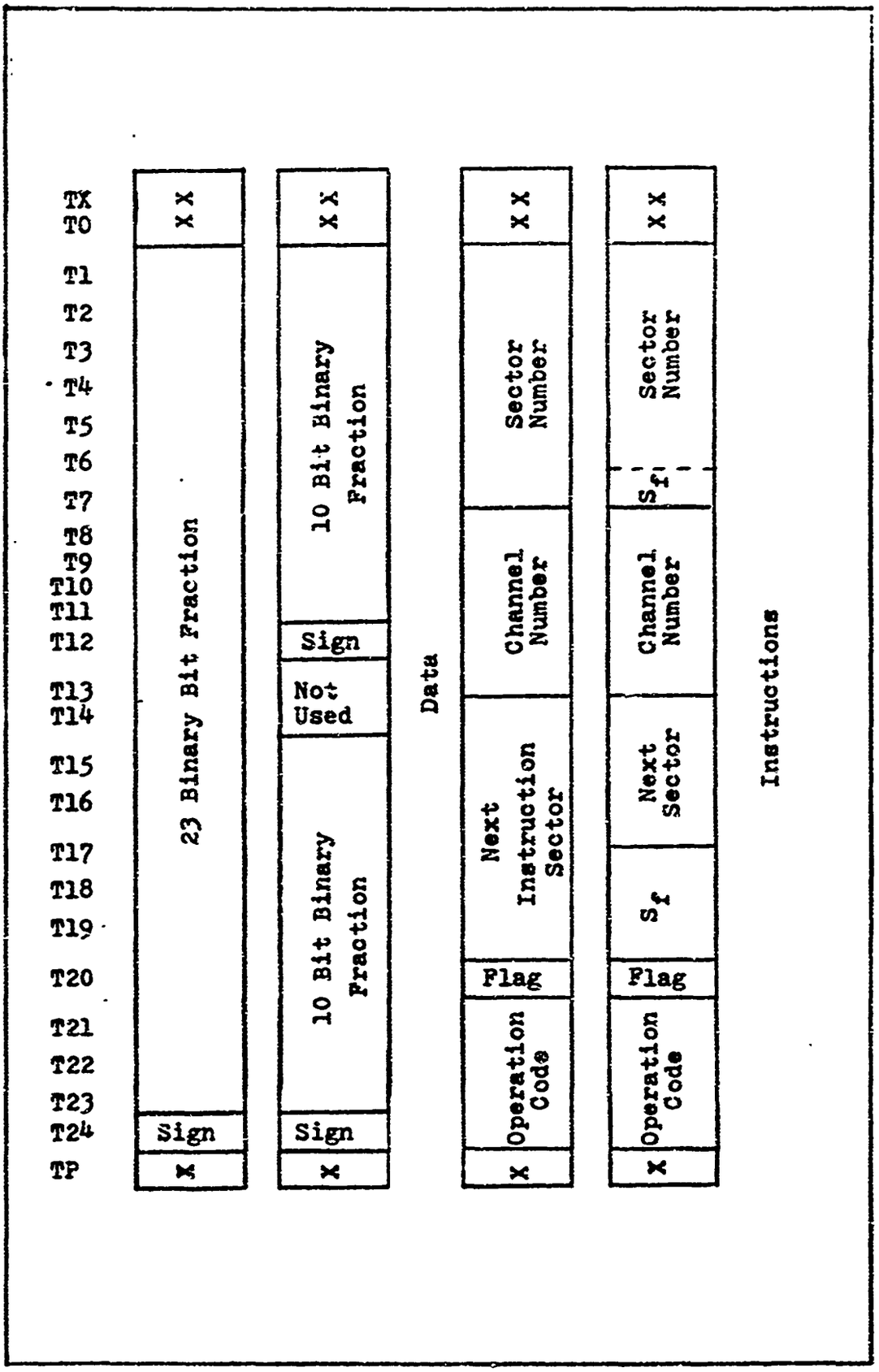


Figure 32. Word Formats.

in Fig. 32. Table VI lists all of the available instructions with numeric and mnemonic codes. For more information on programming see Ref 11.

Table VI.

D37C Computer Instructions

MNEMONIC CODE	DESCRIPTION	NUMERIC CODE	CHANNEL (C) SECTOR (S)
ADD	Add	64	C, S
ALC	Accumulator Left Cycle	00	26, S
ALS	Accumulator Left Shift	00	22, S
ANA	"AND" to Accumulator	40	42, S
ARC	Accumulator Right Cycle	00	36, S
ARS	Accumulator Right Shift	00	32, S
AWC	Add Without Carry	40	50, S
CLA	Clear And Add	44	C, S
COA	Character Output A	00	(40-76), S
COM	Complement	40	46, S
DIA	Discrete Input A	40	02, S
DIB	Discrete Input B	40	00, S
DIC	Discrete Input C	40	20, S
DIV	Divide	34	C, S
DOA	Discrete Output A	40	54, XX2
DOB	Discrete Output B	40	54, XX1
DPP	Disable Platform Power	40	62, X20
ECO	Enable Cable Output	40	62, X02
ECI	Enable Cable Input	40	62, X01
EFC	Enable Fine Countdown	40	26, S
EPP	Enable Platform Power	40	62, X40
FCL	Full Compare and Limit	14	C, S
GBP	Generate Bit Pattern	40	64, S
GPT	Generate Parity Bit	40	60, S
HFC	Halt Fine Countdown	40	24, S
HPR	Halt and Proceed	40	22, S
LPR	Load Phase Register	40	(70-76), S
MAL	Modify A and L	40	52, S
MIM	Minus Magnitude	40	44, S
MPY	Multiply	24	C, S
ORA	"OR" to Accumulator	40	40, S

MNEMONIC CODE	DESCRIPTION	NUMERIC CODE	CHANNEL (C) SECTOR (S)
PLM	Plus Magnitude	40	56, S
RIC	Radio Intercommunication	00	24, 001
RSD	Reset Detector	40	62, X10
SAD	Split Add	60	C, S
SAL	Split Accumulator Left Shift	00	20, S
SAR	Split Accumulator Right Shift	00	30, S
SCL	Split Compare and Limit	04	C, S
SMP	Split Multiply	20	C, S
SPM	Split Plus Magnitude	40	66, S
SRD	Simulate Transient	00	16, S
SSU	Split Subtract	70	C, S
STO	Store Accumulator	54	C, S
SUB	Subtract	74	C, S
TMI	Transfer on Minus	30	C, S
TRA	Transfer	50	C, S
TSM	Transfer Sector on Minus	40	06, S
TSZ	Transfer Sector on Zero	40	04, S
TZE	Transfer on Zero	10	C, S
VIA	Voltage Input A	40	10, S
VIB	Voltage Input B	40	12, S
VIC	Voltage Input C	40	14, S
VID	Voltage Input D	40	16, S
VIE	Voltage Input E	40	30, S
VIF	Voltage Input F	40	32, S
VIG	Voltage Input G	40	34, S
VIH	Voltage Input H	40	36, S

APPENDIX B

Available Computer Signals and Interface Schematics

Appendix B

Available Computer Signals and Interface Schematics

This appendix contains table listings of computer signals available at the connection plugs and schematics of circuits used to interface these signals (Ref 1).

Signals

Table VII. lists all of the signals available at computer interface plugs and gives a description of each. Table VIII. explains the circuit requirements for interfacing each signal as indicated in Table VII. Signals are routed from the computer by the cables as listed in Table IX.

Schematics

The interfacing schematics are divided into output and input circuits. Each group is located on separate circuit boards which simplifies construction and troubleshooting. Parts locations are also given for each board. Most signals are renamed when interfaced and new names are indicated in the wiring lists.

Outputs. All output interfacing circuits are located on circuit board I1. Most signals are converted to TTL levels with IC line receivers, SN75154's. The cable driven outputs are converted using op amps and both the true and complemented signals. Fig. 33 shows the parts locations for I1. Table X lists all of the wiring for the sample receiver circuit illustrated in the table figure. Table XI lists all of the wiring for the sample cable receiver circuit shown in the Table XI

figure.

Inputs. All input interfacing circuits are located on circuit board I2. Most signals are converted to computer levels with IC line drivers, SN75150's. Parts locations are illustratsd in Fig. 36. The data and flag buses are terminated with a pull up resistor, inverter and line driver as shown in Table XIII. The Channel Select lines are interfaced with open collector buffers as shown and listed in Table XIV. A few control signals are interfaced with line drivers only as shown in Table XV. Fig. 40 illustrates the miscellaneous circuits and connections to complete the input board.

Table VII.
D37C Interface Signals

Connector J1

Pin	Term
1	Memory Motor Power 400 cps A ø
2	Memory Motor Power 400 cps B ø
3	Memory Motor Power 400 cps C ø
4	GRD (Computer Common)

Connector J2

Pin	Term	I/O Type	Description
1	X6c	I_1	Discrete Inputs A
2	X7c		
3	X8c		
4	X9c		
5	X12c		
6	X13c		
7	X14c		
8	X17c		
9	X19c		
10	Z15c		Discrete Input C
11	Y1c		Discrete Inputs B
12	Y2c		
13	Y3c		
14	Y4c		
15	Y5c		
16	Y6c		
17	Y7c		
18	Y8c		
19	Y9c		
20	Y10c		
21	Y11c		
22	Y12c		

Table VII.

D37C Interface Signals

Connector J2 (Continued)

Pin	Term	I/O Type	Description
23	Y13c		
24	Y14c		
25	Y15c		
26	Y16c		
27	Y17c		
28	Y18c		
29	Y19c		
30	Y20c		
31	Y21c		
32	Y22c		
33	Y23c		
34	Y24c		
35	Z14c		Discrete Inputs C
36	Z3c		
37	Z4c		
38	Z5c		
39	Z8c		
40	Z9c		
41	Z10c		
42	Z13c		
43	I9c		Incremental Data
44	I10c		
46	V11	I_3	Analog Inputs
47	V12		
48	V13		
49	V14		
50	V38		
51	V37		
53	V21		
54	V22		

Table VII.
D37C Interface Signals

Connector J2 (Continued)

Pin	Term	I/O Type	Description
55	V23		
56	V24		
57	V25		
58	V31		
59	V32		
60	V33		
61	V34		

Connector J3

Pin	Term	I/O Type	Description
1	D07a	O_1	Discrete Outputs A
2	D11a	O_{22}	
3	D12a		
4	D13a	O_1	
5	D14a	O_{22}	
6	D15a		
7	D16a	O_1	
8	D17a	O_{22}	
9	D18a		
10	D19a		
11	D20a		
12	D21a		
13	D22a		
14	D23a		
15	D24a		
16	D25a		
17	D26a		
18	D27a		

Table VII.
D37C Interface Signals

Connector J3 (Continued)

Pin	Term	I/O Type	Description
19	D28a		
20	D29a	O_1	
21	D30a		
22	D31a		
23	D05b		Discrete Outputs B
25	D08b		
26	D10b	O_{22}	
27	D11b		
28	D12b	O_1	
29	D13b	O_{21}	
30	D14b		
32	Z21c	I_1	Discrete Input C
33	SCT1	O_1	Character Output Timing
34	E10	O_{22}	Stage Reference Output
35	E20		
36	E30		
37	Z22c	I_1	Discrete Input C
38	V04a	O_2	Analog Outputs
39	V03a		
40	V02a		
41	V01a		
42	GRD V01	Ground	
43	SVc	O_8	12v LEED Sense
44	X10c	I_1	Discrete Input A
45	Z6c		Discrete Input C
46	CDU0	I_6	Channel Display Select
47	CDU1		
48	CDU2		
49	CDU3		

Table VII.

D37C Interface Signals

Connector J3 (Continued)

Pin	Term	I/O Type	Description
50	CDU4		
51	CDL0		
52	CDL1		
53	CDL2		
54	CDL3		
55	CDL4		
56	GRD VOI	Ground	
57	V41	I_3	Analog Inputs
58	V42		
59	V43		

Connector J4

Pin	Term	I/O Type	Description
1	Ct'	O_3	Clock'
2	Ct		Clock
4	Ot	O_5	Origin Timing
5	Ot'		
7	Ptt		Telemetry Output Timing
8	Ptt'		
10	Axt		Accumulator Monitor
11	Axt'		
13	Et'	O_1	"Enter" Mode Signal
14	Kt'		Compute Mode'
15	Syt'		Synchronization'
16	Mrt	O_7	Master Reset Monitor
17	D15b	O_1	Discrete Output B
18	Irk	I_6	Instruction Read

Table VII.

D37C Interface Signals

Connector J4 (Continued)

Pin	Term	I/O Type	Description
19	V04d	O_2	Analog Outputs
20	V03d		
21	V02d		
22	V01d		
23	Det	O_1	Detector
24	+24 vt	O_{19}	Telemetry Voltage Monitor
25	+18 vt	O_{17}	
26	+12 vt	O_{15}	
27	+9 vt	O_{13}	
28	+6 vt	O_{11}	
29	+3 vt	O_9	
30	-3 vt	O_{10}	
31	-6 vt	O_{12}	
32	-9 vt	O_{14}	
33	-12 vt	O_{16}	
34	-18 vt	O_{18}	
35	-24 vt	O_{20}	
36	Idt	I_7	Initiate Detector
37	Pk	O_1	Parity Error
38	Pvk		Verify Error
39	Q3k		Fill/Verify Mode
40	Mpxk	O_6	Multiplex Channel Display
41	Mpxk'		
43	Ck	O_4	Clock
44	Ck'		
46	Sk	O_6	Sector Track
47	Sk'		
49	Txk		Tx Timing
50	Txk'		

Table VII.
D37C Interface Signals

Connector J4 (Continued)

Pin	Term	I/O Type	Description
51	V15t	I_3	Not Used
52	Nmhk	O_1	Manual Halt Mode
53	Phk	O_{22}	Program Halt Mode
54	V16t	I_3	Not Used
55	Ksk'	I_2	Single Cycle'
56	Krk'	I_7	Run'
57	V17t	I_3	Not Used
58	Tc	I_2	Load Clock
59	Fsc	I_1	Initiate Load
60	Bxk	O_6	Disturbance Monitor
61	Bxk'		

Connector J5

Pin	Term	I/O Type	Description
1	X1c	I_1	Discrete Inputs A
2	X2c		
3	X3c		
4	X4c		
5	X5c		
6	Z17c		Discrete Inputs C
7	Z18c		
8	Z2c		
10	I8c		Incremental Input
12	I1c		Character Inputs
13	I2c		
14	I3c		
15	I4c		
16	I5c		

Table VII.
D37C Interface Signals

Connector J5 (Continued)

Pin	Term	I/O Type	Description
17	Tc'	I_4	Load Clock
18	ZD	O_1	Zero Discrete
19	Mrc	I_7	Master Reset
20	Khc'		Halt'
21	Ewc	I_5	Write Enable
22	RAc	I_1	Radio Control
23	RTc		
25	RSc		
26	CAc		Cable Control
27	CTc	I_7	
28	ROc	O_1	Radio Status
29	COc		Cable Status
30	CRc		Radio/Cable Status
32	D09a	O_{23}	Discrete Output A
33	D09b		Discrete Output B
35	SC10	O_1	Character Output
36	SC20		
37	SC30		
38	SC40		
39	SC50		
40	SCT0		
41	Z19c	I_1	Discrete Input C
42	Kc	O_1	Compute Mode
43	Lkc		Load Mode
44	Pvec		Verify/Parity Error
46	Z24c	I_1	Discrete Input C
47	D00a	O_1	Discrete Output A
48	D01a		
49	D02a		
50	D03a		

Table VII.
D37C Interface Signals

Connector J5 (Continued)

Pin	Term	I/O Type	Description
51	D04a		
52	D05a		
53	D06a		
54	D08a		
55	D10a		
56	D01b		Discrete Outputs B
57	D02b		
58	D03b		
59	D04b		
60	D06b		
61	D07b		

Connector J6

Pin	Term	I/O Type	Description
1	X11c	I_1	Discrete Inputs A
2	X15c		
3	X16c		
4	X18c		
5	X20c (Ib)		
6	Z16c		Discrete Inputs C
8	Z7c		
9	Z11c		
10	Z12c		
12	I1 ac		Incremental Inputs
13	I1 bc		
14	I2 ac		
15	I2 bc		
16	I3 ac		
17	I3 bc		

Table VII.

D37C Interface Signals

Connector J6 (Continued)

Pin	Term	I/O Type	Description
18	I4 ac		
19	I4 bc		
20	I5 ac		
21	I5 bc		
22	I6 ac		
23	I6 bc		
24	I7 ac		
25	I7 bc		
27	V15	I_3	Analog Inputs
28	V16		
29	V17		
30	V18		
31	V45		Analog Inputs
32	V26		
33	V27		
34	V28		
35	V35		
36	V36		
37	V44		
38	V46		
39	V47		
40	V48		
41	E00	O_1	Platform Power Enable
43	G10c		Gyro Torque Control
44	G11c		
45	G20c		
46	G21c		
47	G30c		
48	G31c		

Table VII.
D37C Interface Signals

Connector J6 (Continued)

Pin	Term	I/O Type	Description
49	G40c		
50	G41c		
53	V04b	O_2	Analog Outputs
54	V04c		
55	V03b		
56	V03c		
57	V02b		
58	V02c		
59	V01b		
60	V01c		

Connector J7

Pin	Term
1	+28 Volts DC Primary Power
2	+28 Volts DC Primary Power
3	GRD (+28V Return)
4	GRD (+28V Return)

Connector J8

Pin	Term	I/O Circuit Type
1	+9 MT	+9V Marginal Test
2	GND	Signal Ground
3	+6 MT	+6V Marginal Test
4	MPXA	Mpxa Enable and Disable Monitor
5	+3 MT	+3V Marginal Test
6	+18 MT	+18V Marginal Test

Table VII.

D37C Interface Signals

Connector J8 (Continued)

Pin	Term	I/O Circuit Type
7	+24 MT	+24V Marginal Test
8	-24 CSN	-24V Current Sense Negative
9	+24 FTO	+24V Functional Test Turn-Off
10	+12 CSN	+12V Current Sense Negative
11	+9 FTO	+9V Functional Test Turn-Off
12	+3 CSP	+3V Current Sense Positive
13	-9 M	-9V Monitor
14	+6 CSN	+6V Current Sense Negative
15	+18 FTP	+18V Functional Test Turn-Off
16	+24 CSN	+24V Current Sense Negative
17	-24 MT	-24V Marginal Test
18	-18 MT	-18V Marginal Test
19	-24 FTO	-24V Functional Test Turn-Off
20	-12 FTO	-12V Functional Test Turn-Off
21	+12 MT	+12V Marginal Test
22	-18 CSP	-18V Current Sense Positive
23	+12 FTO	+12V Functional Test Turn-Off
24	+18 CSP	+18V Current Sense Positive
25	+18 CSN	+18V Current Sense Negative
26	-3 CSN	-3V Current Sense Positive
27	+3 FTO	+3V Functional Test Turn-Off
28	+6 CSP	+6V Current Sense Positive
29	-3 M	-3V Monitor
30	-6 CSP	-6V Current Sense Positive
31	-6 CSN	-6V Current Sense Negative
32	-6 MT	-6V Marginal Test
33	-12 MT	-12V Marginal Test
34	-9 MT	-9V Marginal Test
35	+24 CSP	+24V Current Sense Positive
36	-18 FTO	-18V Functional Test Turn-Off

Table VII.

D37C Interface Signals

Connector J8 (Continued)

Pin	Term	I/O Circuit Type
37	-12 CSN	-12V Current Sense Negative
38	+9 CSP	+9V Current Sense Positive
39	-24 CSP	-24V Current Sense Positive
40	-18 CSN	-18V Current Sense Negative
41	C6K	Operand Memory Bank 0_{22}
42	C7K	Operand Memory Bank 0_{22}
43	-3 MT	-3V Marginal Test
44	CP6K	Program Memory Bank 0_{22}
45	CP7K	Program Memory Bank 0_{22}
46	+12 CSP	+12V Current Sense Positive
47	+3 CSN	+3V Current Sense Negative
48	-3 CSN	-3V Current Sense Negative
49	-6 FTO	-6V Functional Test Turn-Off
50	-12 M	-12V Monitor
51	-24 M	-24V Monitor
52	-6 M	-6V Monitor
53	+6 FTO	+6V Functional Test Turn-Off
54	-9 CSP	-9V Current Sense Positive
55	-12 CSP	-12V Current Sense Positive
56	-3 FTO	-3V Functional Test Turn-Off
57	INVFTO	Inverter Functional Test Turn-Off
58	-28 RFI	-28V RFI Negative
59	-9 FTO	-9V Functional Test Turn-Off
60	-9 CSN	-9V Current Sense Negative
61	+9 CSN	+9V Current Sense Negative

Connector J9

Pin	Term	Description
1	Mpx	Mpx Enable and Disable

Table VII.
D37C Interface Signals

Connector J9 (Continued)

Pin	Term	Description
2	Mpxa	See Chapter III.
3	GND	
4	GND	

Table VIII.

Signal Requirements for I/O Types

Inputs

Type		Requirements
Type I_1	True Level	-15 (+11,-12) vdc input shall be provided to a current source having a positive output current equal to or less than 1.5 ma and a parallel resistance greater than 100 K ohms.
	False Level	+12 ±8 vdc input or an open circuit shall be provided to a resistance greater than 100 K ohms.
Type I_2	True Level	Same as I_1 False
	False Level	Same as I_1 True
Type I_3		+11.5 to -11.5 vdc input shall be provided through a source resistance between 0 and 5.5 K ohms; current drain on input shall be equal to or less than 11.5 μa.
Type I_4	True Level	-14 (+14, -13) vdc input or an open circuit shall be provided to a resistance greater than 1 megohm.
	False Level	+14 (+10, -11) vdc input shall be provided to a current source having a positive input current equal to or less than 2.0 ma and a parallel greater than 100 K ohms.
Type I_5	True Level	+31 (+8, -9) vdc input shall be provided to a 14 to 20 K ohm resistance in series with a +5.0 to +7.3 vdc source.
	False Level	Open circuit shall be provided to a 14 to 20 K ohm resistance in series with a +4.5 to +6.0 vdc source.
Type I_6	True Level	+6.0 ± 0.5 vdc input shall be provided to a resistance greater than 100 K ohms.

Table VIII.

Signal Requirements for I/O Types (Continued)

	False Level	+0.4 (+0.3, -0.4) vdc input shall be provided to a current source having a positive output current equal to or less than 7.5 ma and 1.04 K ohms parallel resistance.
Type I_7	True Level	-15 (+11, -12) vdc shall be provided to a current source having a positive 2.8 ma and a parallel resistance greater than 20 K ohms.
	False Level	+12 ±8 vdc input or an open circuit shall be provided to a +6 ±0.5 vdc source through a series resistance of 27.4 K ohms +5%.

Outputs

Type		Voltage Level VDC	Output Resistance Ohms	Max Current ma
O_1	True	-12 ± 0.8	375 ± 225	≤8 in
	False	+6 ± 0.5	375 ± 225	≤8 out
O_2		+10.0 ± 0.20 to -10.0 ± 0.20	Output Resistance = 2K ± 1% to ground	≤6 *
O_7	True	+5 (+.5, -1.0)	1010 ± 50	≤3.5 out
		+0.4 ± 0.4	<50	≤15 in
O_8**		-10 (+1, -2)	1.0 ± 0.1 K	<8 in
O_{21}	True	-12 ± 0.8	<20	≤110 in
	False	+6 ± 0.5	4.7K	
O_9		+3 ± 0.15	1000 ± 1	≤7.9 out

Table VIII.

Signal Requirements for I/O Types (Continued)

Type		Voltage Level VDC	Output Resistance Ohms	Max Current ma
O_{10}		-3 ± 0.15	1500 ± 1	≤6.4 in
O_{11}		+6 ± 0.3	1100 ± 1	≤7.5 out
O_{12}		-6 ± 0.3	2200 ± 1	≤5.3 in
O_{13}		+9 ± 0.9	2000 ± 1	≤5.5 out
O_{14}		-9 ± 0.9	3000 ± 1	≤4.5 in
O_{15}		+12 ± 0.6	2900 ± 1	≤4.6 out
O_{16}		-12 ± 0.6	3800 ± 1	≤4.0 in
O_{17}		+18 ± 1.8	4700 ± 2	≤3.6 out
O_{18}		-18 ± 1.8	5400 ± 2	≤3.4 in
O_{19}		+24 ± 2.4	6500 ± 2	≤3.1 out
O_{20}		-24 ± 2.4	7200 ± 3	≤2.9 in
O_{22}	True	-8.2 to -12.8	The outputs of this circuit must be terminated in an impedance of 1.05 megohm or less	≤6.5 in
	False	+2.5 to +6.5		≤1.7 out
O_{23}**	True	-8.0 to -12.0	1.2K ± 0.3K	≤5 in
		+3.5 to +6.5	1.15K ± 0.85K	≤1.7 out

**The outputs of this circuit are protected against shorts to a maximum of ±29.7 volts dc.

*The circuit shall supply or accept this current depending upon polarity.

Table VIII.

Signal Requirements for I/O Types (Continued)

Cable Drivers

All cable drivers are designed to drive a cable with 75 ohm characteristic impedance connected to a load of 37.5 ohms $\pm$ 5% and $\pm 6 \pm 0.75$ volts.

Type		Description
O_3	True	27 ± 5 ma sink
	False	$\geq$ 10K resistance
O_4	True	13 (-2, +3) ma sink
	False	$\geq$ 10K resistance
O_5	True	29 ± 6 ma sink
	False	$\geq$ 10K resistance
O_6	True	14.5 ± 3.0 ma sink
	False	$\geq$ 10K resistance

Table IX.
Computer Cable Wiring List

Pin	Func	Pin	Pin	Func	Pin
J1-1	AØ	PDU	J2-48	13	SDU
2	BØ	"	49	14	"
3	CØ	"	50	38	"
4	Gnd	"	51	37	"
			53	21	"
J2-11	Y1c	I2-34-8	54	22	"
12	2	9	55	23	"
13	3	7	56	24	"
14	4	10	57	V25	"
15	5	6	58	31	"
16	6	11	59	32	"
17	7	5	60	33	"
18	8	12	61	34	"
19	9	4			
20	10	13	J3-1	D07a	I1-4-8
21	11	3	2	11	9
22	12	14	3	12	7
23	13	2	4	13	10
24	14	15	5	14	6
25	15	1	6	15	11
26	16	16	7	16	5
27	17	I2-35-1	8	17	12
28	18	2	9	18	4
29	19	3	10	19	13
30	20	4	11	20	3
31	21	5	12	21	14
32	22	6	13	22	2
33	23	7	14	23	15
34	24c	8	15	24	1
46	V11	SDU	16	25	16
47	12	"	17	26	I1-3-8

Table IX.

Computer Cable Wiring List (Continued)

Pin	Func	Pin	Pin	Func	Pin
J3-18	D27a	I1-3-9	J3-56	GRD V01	SDU
19	28	7	57	V41	"
20	29	10	58	42	"
21	30	6	59	V43	"
22	31a	11			
23	D05b	5	J4-1	Ct'	I1-3
24	No Conn	12	2	Ct	4
25	D08b	4	4	Ct	5
26	10	13	5	Ot'	6
27	11	3	7	Ptt	8
28	12	14	8	Ptt'	9
29	13	2	10	Axt	10
30	14	15	11	Axt'	11
34	E10	1	13	Et'	I1-2-2
35	E20	16	14	Kt'	3
36	E30	I1-2-1	15	Syt'	4
38	V04a	SDU	16	Mrt	5
39	03	"	17	D15b	6
40	02	"	18	Irk	I2-3
41	01	"	19	V04d	SDU
42	GRD V01	"	20	03	"
46	CDU 0	I2-35-9	21	02	"
47	1	10	22	01	"
48	2	11	24	+24vt	"
49	3	12	25	+18vt	"
50	4	13	26	+12vt	"
51	CDL 0	14	27	+ 9vt	"
52	1	15	28	+ 6vt	"
53	2	16	29	+ 3vt	"
54	3	I2-1	30	- 3vt	"
5	4	2	31	- 6vt	"

Table IX.

Computer Cable Wiring List (Continued)

Pin	Func	Pin	Pin	Func	Pin
J4-32	- 9vt	SDU	J5-18	ZD	
33	-12vt	"	19	Mrc	CP
34	-18vt	"	20	Khc'	I2-18
35	-24vt	"	21	Ewc	CP
37	Pk	I1-2-7	32	D09a	I1-2-12
38	Pvk	8	33	D09b	13
39	03k	9	42	Kc	14
40	Mpxk	I1-13	43	Lkc	15
41	Mpxk'	14	44	Pvec	I1-1-8
46	Sk	15	47	D00a	9
47	Sk'	16	48	01	7
49	Txk	18	49	02	10
50	Txk'	19	50	03	6
52	Nmhk	I1-2-10	51	04	11
53	Phk	11	52	05	5
55	Ksk'	I2-4	53	06	12
56	Krk'	I2-5	54	08	4
58	Tc	6	55	10	13
59	Fsc	CP	56	D01b	3
			57	02	14
J5-1	X1c	I2-7	58	03	2
2	2	8	59	04	15
3	3	9	60	06	1
4	4	10	61	07	16
5	5	11			
12	I1C	12	J6-27	V15	SDU
13	2	13	28	16	"
14	3	14	29	17	"
15	4	15	30	18	"
16	5	16	31	45	"
17	Tc'	17	32	26	"

Table IX.

Computer Cable Wiring List (Continued)

Pin	Func	Pin
J6-33	V27	SDU
34	28	"
35	35	"
36	36	"
37	44	"
38	46	"
39	47	"
40	48	"
41	E00	I1-2-16
53	V04b	SDU
54	04c	"
55	03b	"
56	03c	"
57	02b	"
58	02c	"
59	01b	"
60	01c	"
J7-1	+28	PDU
2	+28	"
3	6	"
4	6	"
J8-2	G	
4	Mpxa	SDU
41	C6k	I1-5-1
42	C7k	2
44	CP6k	3
45	CP7k	4
J9-1	Mpx	J9-2

Pin	Func	Pin
J9-2	Mpxa	-1
3	No Conn	
4	No Conn	

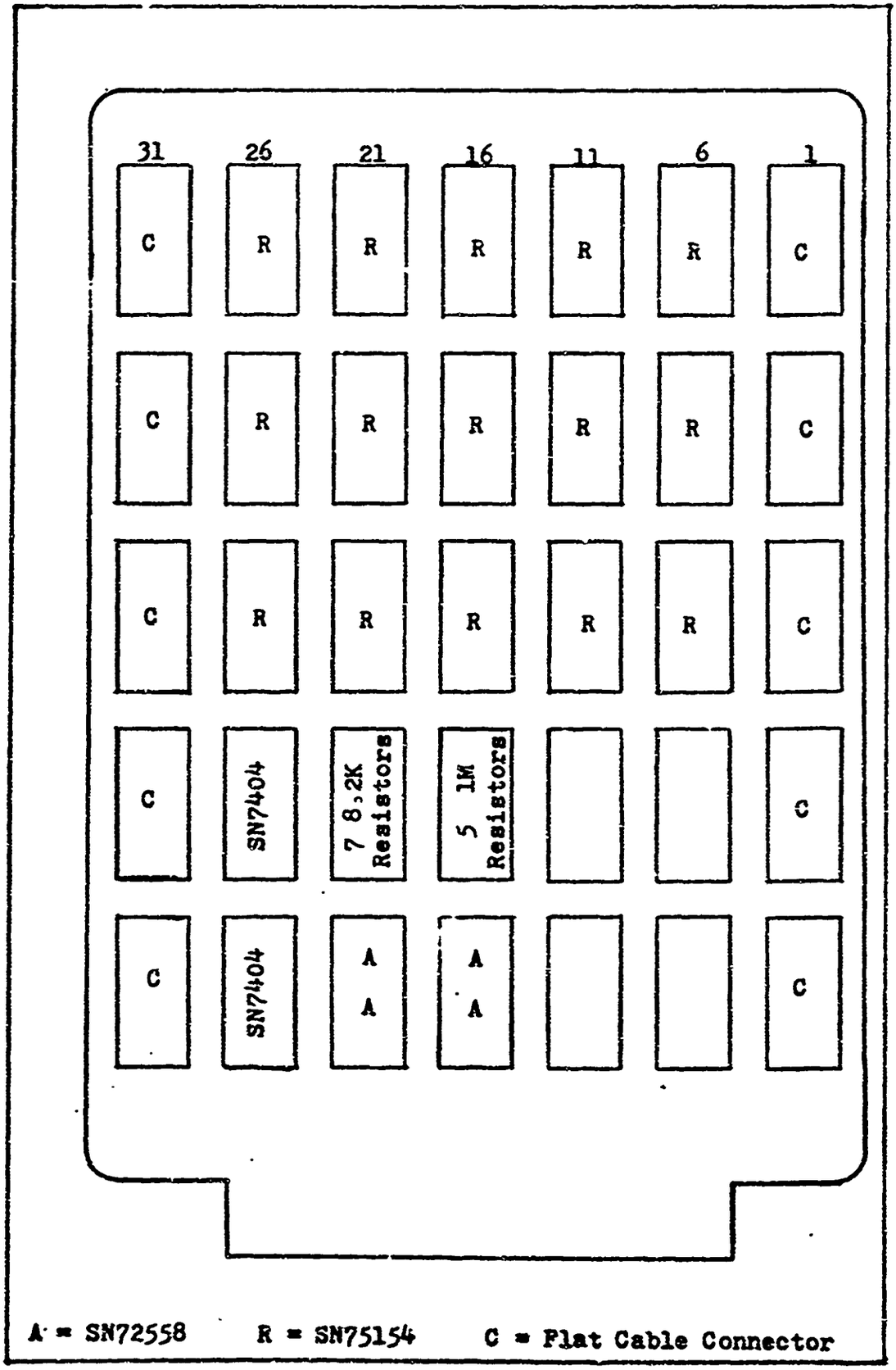


Figure 33. I1 Parts Location.

Table X.

Signal Receiver Circuits

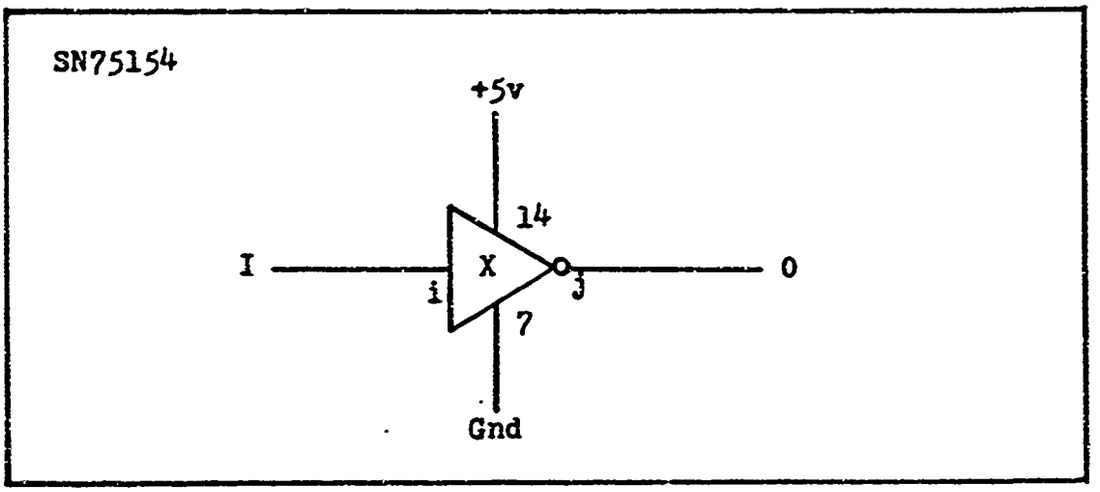


Figure 34. Sample Receiver Circuit.

Term	I	X	i	j	O	Term
D06b	I1-1-1	6	3	12	I1-32-6	C6
D03b	2		4	11	3	3
D01b	3		5	10	1	1
D08a	4		6	9	34-9	DS8
D05a	5	11	3	12	6	5
D03a	6		4	11	4	3
D01a	7		5	10	2	1
Pvec	8		6	9		
D00a	9	16	3	12	34-1	DS0
D02a	10		4	11	3	2
D04a	11		5	10	5	4
D06a	12		6	9	7	6
D10a	13	21	3	12	11	10
D02b	14		4	11	32-2	C2
D04b	15		5	10	4	4
D07b	16		6	9	7	7
D19a	4-13	26	3	12	33-4	DS19
D21a	14		4	11	6	21
D23a	15		5	10	8	23

Table X.

Signal Receiver Circuits (Continued)

Term	I	X	i	j	0	Term
Syt'	I1-2-4		6	9	I1-31-4	Ms'
Mrt	5	7	3	12	14	Mrt'
D15b	6	7	4	11	15	C15
Pk	7		5	10	31-2	Ep
Pvk	8		6	9	3	Ev
03k	9	12	3	12	10	Mv
Nmhk	10		4	11	5	Mmh
Phk	11		5	10	6	Mph
D09a	12		6	9	34-10	DS9
D09b	13	17	3	12	32-9	C9
Kc	14		4	11	31-7	Mc
Lkc	15		5	10	8	M1
E00	16		6	9	9	IGP
		22	3	12		
D13b	3-2		4	11	32-13	C13
D11b	3		5	10	11	11
D08b	4		6	9	8	8
D05b	5	27	3	12	5	5
D30a	6		4	11	33-15	DS30
D28a	7		5	10	13	28
D26a	8		6	9	11	26
D27a	9	8	3	12	12	27
D29a	10		4	11	14	29
D31a	11		5	10	16	31
D25a	4-16		6	9	10	25
D10b	3-13	13	3	12	32-10	C10
D12b	14		4	11	12	12
D14b	15		5	10	14	14
			6	9		
D24a	4-1	18	3	12	33-9	DS24
D22a	2		4	11	7	22

Table X.

Signal Receiver Circuits (Continued)

Term	I	X	i	j	0	Term
D20a	I1-4-3		5	10	I1-33-5	DS20
D18a	4		6	9	3	18
D16a	5	23	3	12	1	16
D14a	6		4	11	34-15	14
D12a	7		5	10	13	12
D07a	8		6	9	8	7
D11a	9	28	3	12	12	11
D13a	10		4	11	14	13
D15a	11		5	10	16	15
D17a	12		6	9	33-2	17

Table XI.

Cable Interface Circuits

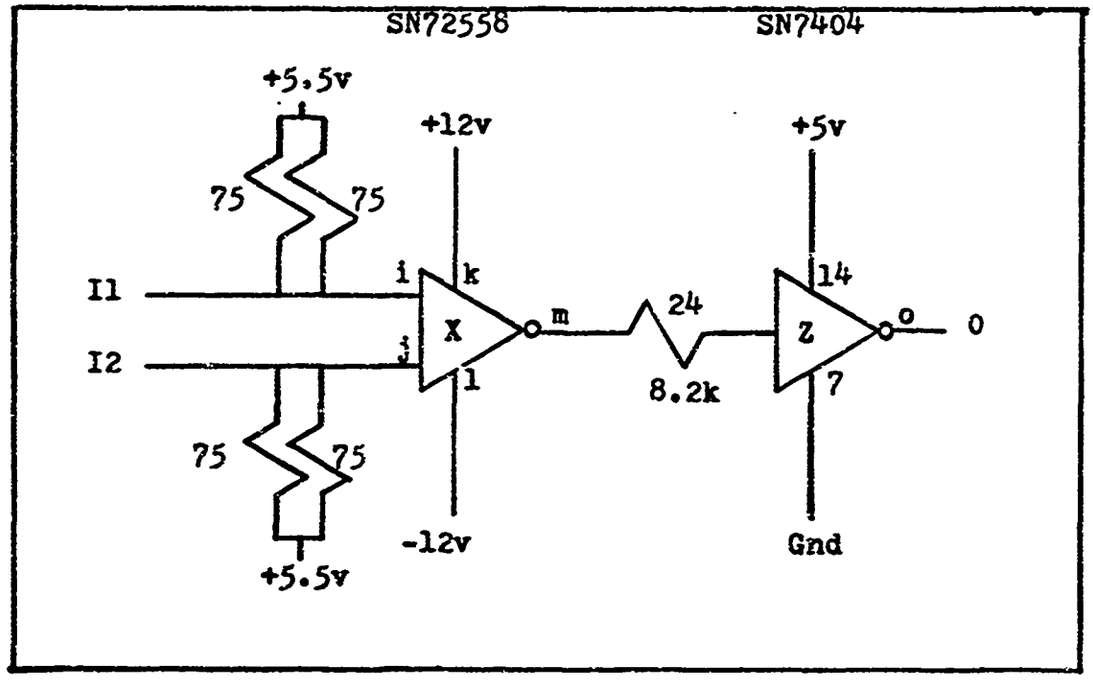


Figure 35. Sample Cable Receiver.

I1	I2	X	i	j	k	l	m	Z	n	o	0	Term
I1-3	I1-4	25	2	3	16	4	1	29	1	2	I1-31-1	Ck
5	6		13	14			15		3	4	31-11	Ot
8	9		7	6	12	8	5		5	6	12	Ptt
10	11		9	10			11		9	8	13	Axt
13	14	20	3	2	16	4	1		11	10	35-1	Mpx
15	16		13	14			15		13	12	3	Sk
18	19		7	6	12	8	5	30	1	2	2	Txk

Miscellaneous I1 Connections

Term	Pin	to	Pin
E10	I1-3-1		I1-19-1
E20	16		2

Table XI.
Cable Interface Circuits

Miscellaneous I1 Connections (Continued)

Term	Pin	to	Pin
E30	2-1		3
Mc	31-7		I1-21
Ck	31-1		32-16
+5.5v	I1-2		
	B		
GND	I1-22		
	Z		
+12v	I1-X		
-12v	I1-Y		

Table XII.

Cable List from I1

Pin	Func	Pin	Pin	Func	Pin
I1-31-1	Ck	A-5-1	I1-32-15	C15	SDU
2	Ep	2	16	Ck	"
3	Ev	3			
4	Ms'	4	I1-33-1	DS16	SDU
5	Mmh	5	2	17	"
6	Mph	6	3	18	"
7	Mc	7	4	19	"
8	Ml	8	5	20	"
9	IOP	9	6	21	"
10	Mv	10	7	22	"
11	Ot	11	8	23	"
12	Pt	12	9	24	"
13	Ac	13	10	25	"
14	Mrt	14	11	26	"
15	Spare	15	12	27	"
16	Spare	16	13	28	"
			14	29	"
I1-32-1	C1	SDU	15	30	"
2	2	"	16	31	"
3	3	"			
4	4	"	I1-34-1	DS0	SDU
5	5	"	2	1	"
6	6	"	3	2	"
7	7	"	4	3	"
8	8	"	5	4	"
9	9	"	6	5	"
10	10	"	7	6	"
11	11	"	8	7	"
12	12	"	9	8	"
13	13	"	10	9	"
14	14	"	11	10	"

Table XII.

Cable List from I1 (Continued)

Pin	Func	Pin
I1-34-12	DS11	SDU
13	12	"
14	13	"
15	14	"
16	15	"
I1-35-1	Mpx	P-
2	Tx	
3	Sk	
4	BP1	
5	BP2	
6	B01	
7	B02	
8	Spare	
9	"	
10	"	
11	"	
12	"	
13	"	
14	"	
15	"	
16	"	
I1-21	Mc	I2-M

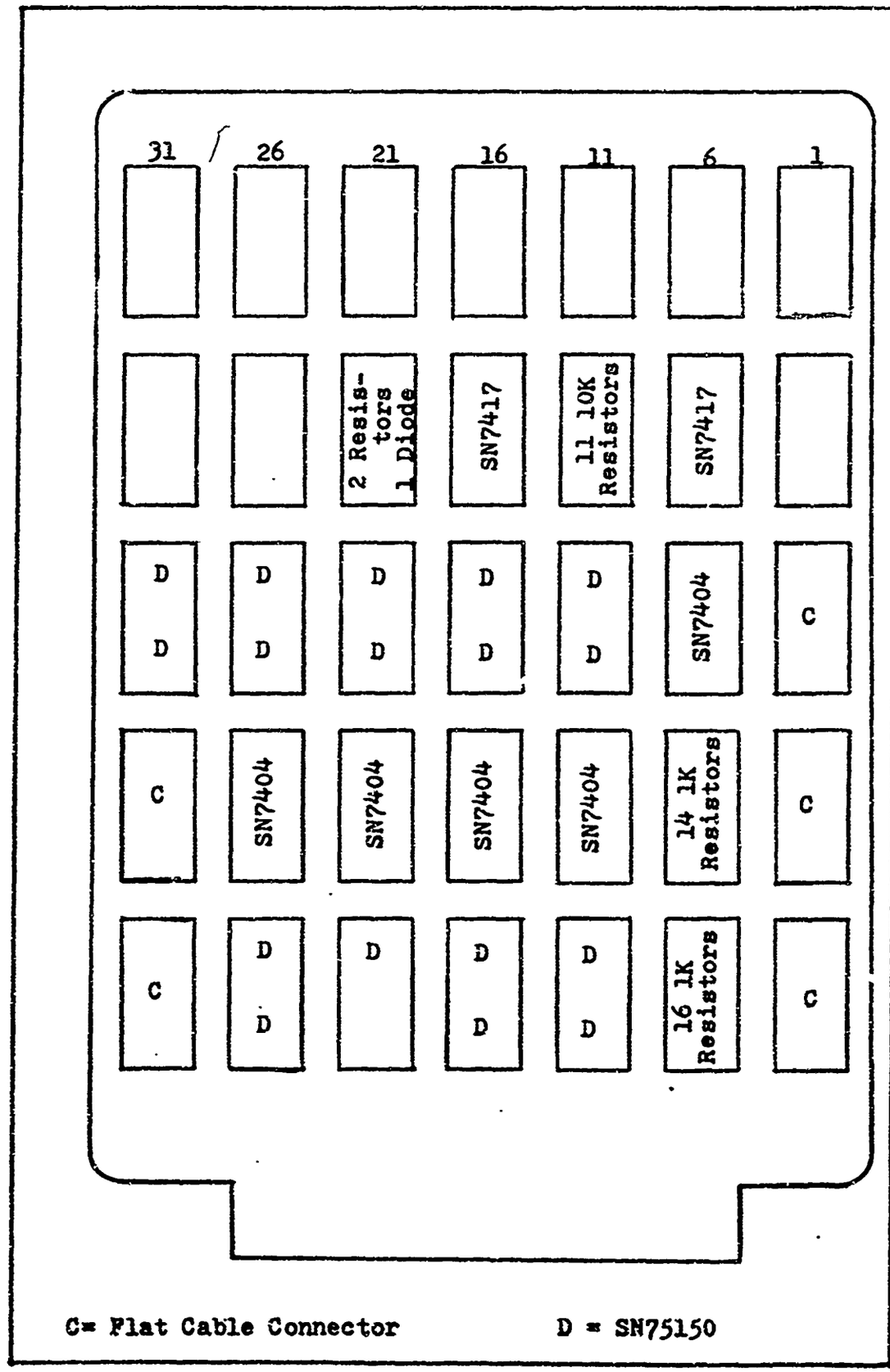


Figure 36. I2 Parts Location.

Table XIII.

Bus and Flag Interfacing

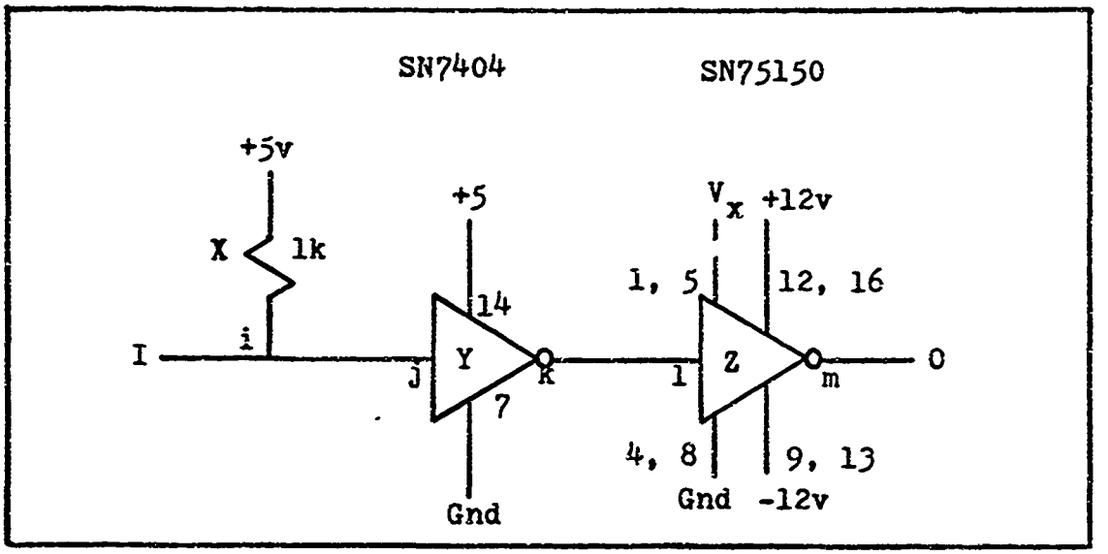


Figure 37. Sample Bus Interfaces.

Term	I	X	i	Y	j	k	Z	1	m	O	Term
D1	I2-5-1	9	1	8	1	2	13	2	15	I2-34-8	Y1C
2	2		2		3	4		3	14	9	2
3	3		3		5	6		6	11	7	3
4	4		4		9	8		7	10	10	4
5	5		5		11	10	15	2	15	6	5
6	6		6		13	12		3	14	11	6
7	7		7	14	1	2		6	11	5	7
8	8		8		3	4		7	10	12	8
9	9		9		5	6	18	2	15	4	9
10	10		9		9	8		3	14	13	10
11	11		11		11	10		6	11	3	11
12	12		12		13	12		7	10	14	12
13	13		13	19	1	2	20	2	15	2	13
14	14		14		3	4	23	2	15	15	14
15	15	10	1		5	6		3	14	1	15
16	16		2		9	8		6	11	16	16
17	I2-4-1		3		11	10		7	10	I2-35-1	17
18	2		4		13	12	28	2	15	2	18

Table XIII.

Bus and Flag Interfacing (Continued)

Term	I	X	i	Y	j	k	Z	l	m	O	Term
D19	I2-4-3		5	24	1	2		3	14	I2-35-3	Y19C
20	4		6		3	4		6	11	4	20
21	5		7		5	6		7	10	5	21
22	6		8		9	8	30	2	15	6	22
23	7		9		11	10		3	14	7	23
24	8		10		13	12		6	11	8	24
F1	I2-E		11	29	1	2		7	10	I2-7	X1C
2	F		12		3	4	33	2	15	8	2
3	H		13		5	6		3	14	9	3
4	J		14		9	8		6	11	10	4
5	K		15		11	10		7	10	11	5

Table XIV.
Channel Select Circuits

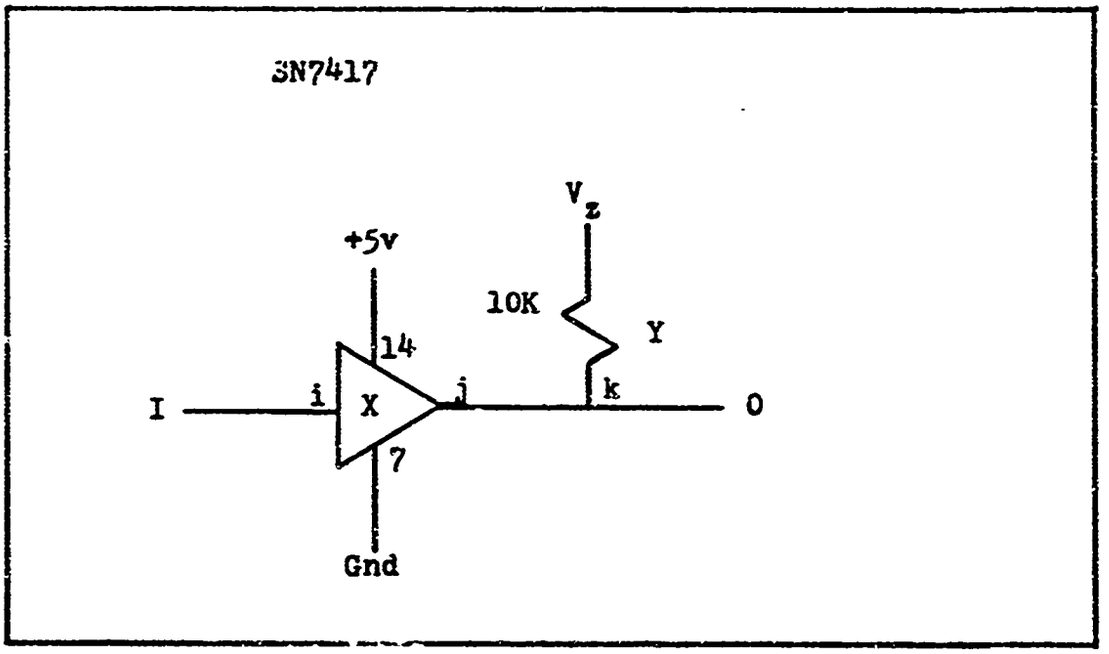


Figure 38. Sample Channel Driver.

Term	I	X	i	j	Y	R	0	Term
Cu0'	I2-4-11	7	1	2	12	1	I2-35-9	Cdu0
1'	12		3	4		2	10	1
2'	13		5	6		3	11	2
3'	14		9	8		4	12	3
4'	15		11	10		5	13	4
C10'	16		13	12		6	14	Cd10
1'	I2-N	17	1	2		7	15	1
2'	P		3	4		8	16	2
3'	R		5	6		9	I2-1	3
4'	S		9	8		10	2	4
IRK'	M		11	10		11	3	IRK

Table XV.

Control Signal Interface

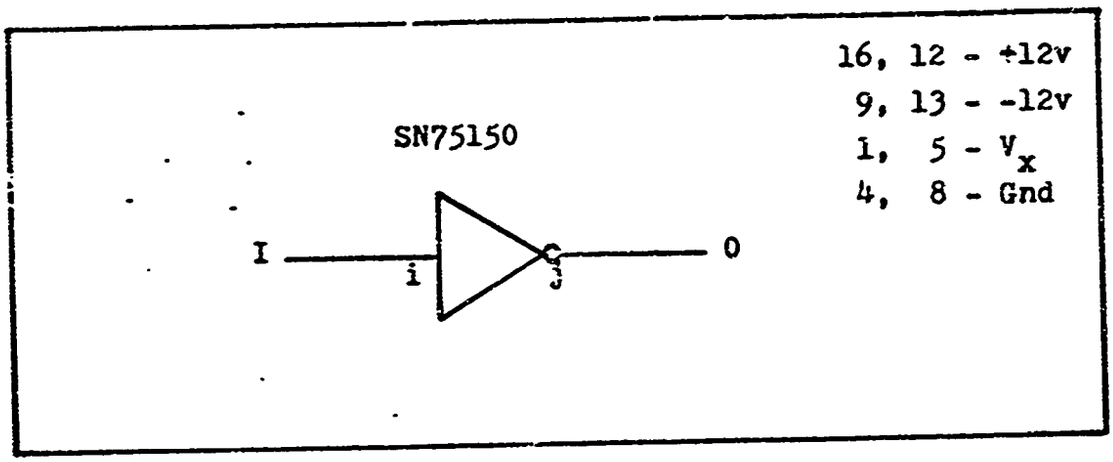


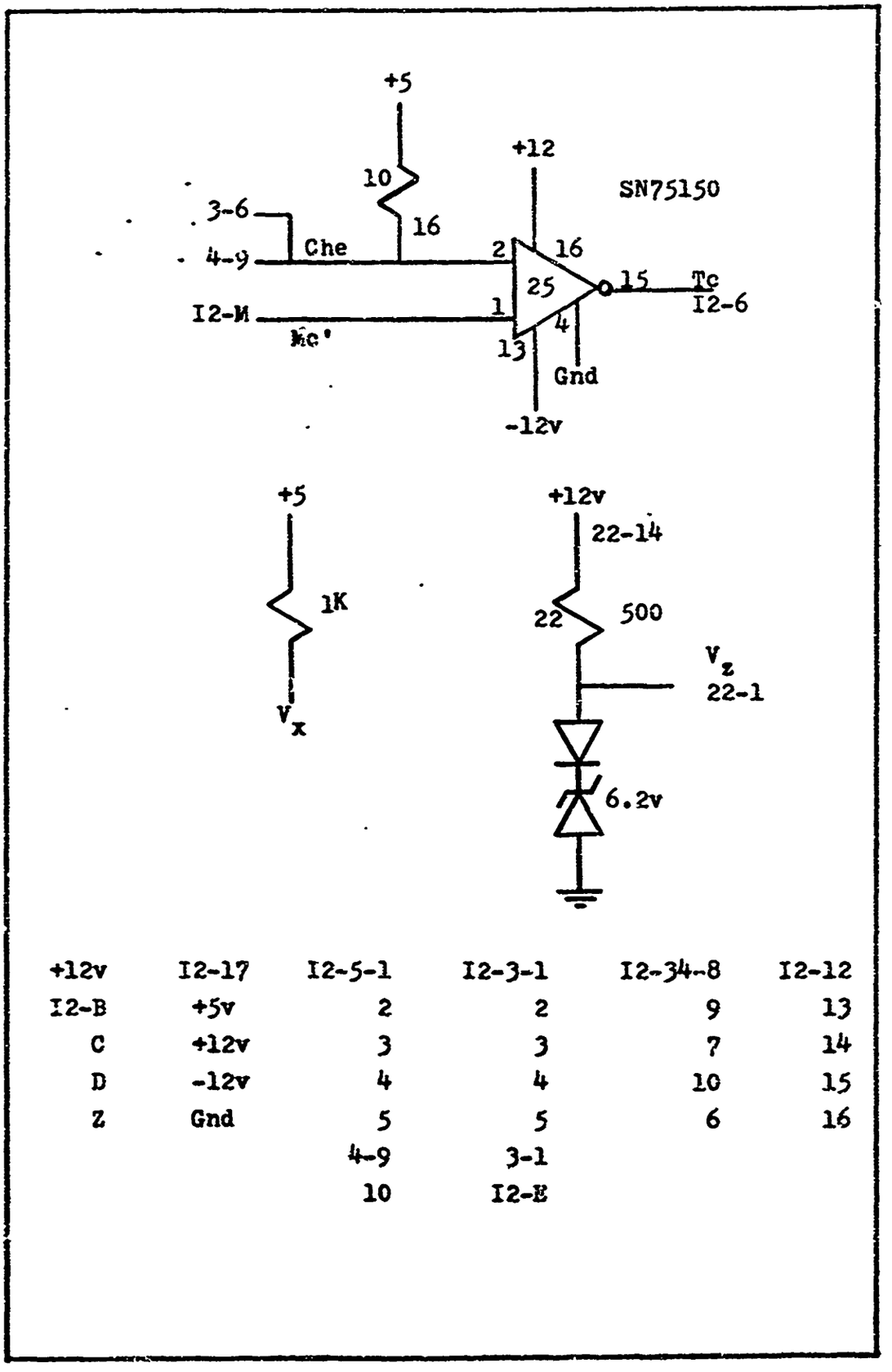
Figure 39. Sample Control Interface.

I	X	i	j	O	Input	Output
I2-T	20	3	14	I2-4	SS	Ksk'
U		6	11	5	Rn'	Krk'
V		7	10	18	Hlt'	Khc'

Table XVI.

Cable List to I2

Pin	Func	Pin	Pin	Func	Pin
I2-3-1	D1	P	I2-5-1	D1	A-1
2	2		2	2	2
3	3		3	3	3
4	4		4	4	4
5	5		5	5	5
6	Che		6	6	6
7	Rn'		7	7	7
8	Ss		8	8	8
9	Hlt		9	9	9
10	Spare		10	10	10
11			11	11	11
12			12	12	12
13			13	13	13
14			14	14	14
15			15	15	15
16			16	16	16
I2-4-1	D17	A-17	I2-A	No Conn	
2	18	18	B	+ 5.5	PDU
3	19	19	C	+12v	"
4	20	20	D	-12v	"
5	21	21	E	F1	SDU
6	22	22	F	2	"
7	23	A-C	H	3	"
8	24	D	J	4	"
9	Che	E	K	5	"
10	F1	F	L	None	
11	Cu0	J	M	Mc'	I1-21
12	1	K	N	C11	A-S
13	2	L	P	2	T
14	3	M	R	3	U
15	4	P	S	4	V
16	C10	R	Z	Gnd	PDU



+12v	I2-17	I2-5-1	I2-3-1	I2-34-8	I2-12
I2-B	+5v	2	2	9	13
C	+12v	3	3	7	14
D	-12v	4	4	10	15
Z	Gnd	5	5	6	16
		4-9	3-1		
		10	I2-E		

Figure 40. Miscellaneous Input Circuits and Connections.

APPENDIX C

System Schematics

Appendix C

System Schematics

This appendix contains the remaining schematics needed to construct and troubleshoot the converted D37C system. The PDU and SDU drawings are repeated in this section as a conveinence to the reader. The rest consists of figures defining the panel circuit board, PB, and circuit board A in the card chassis.

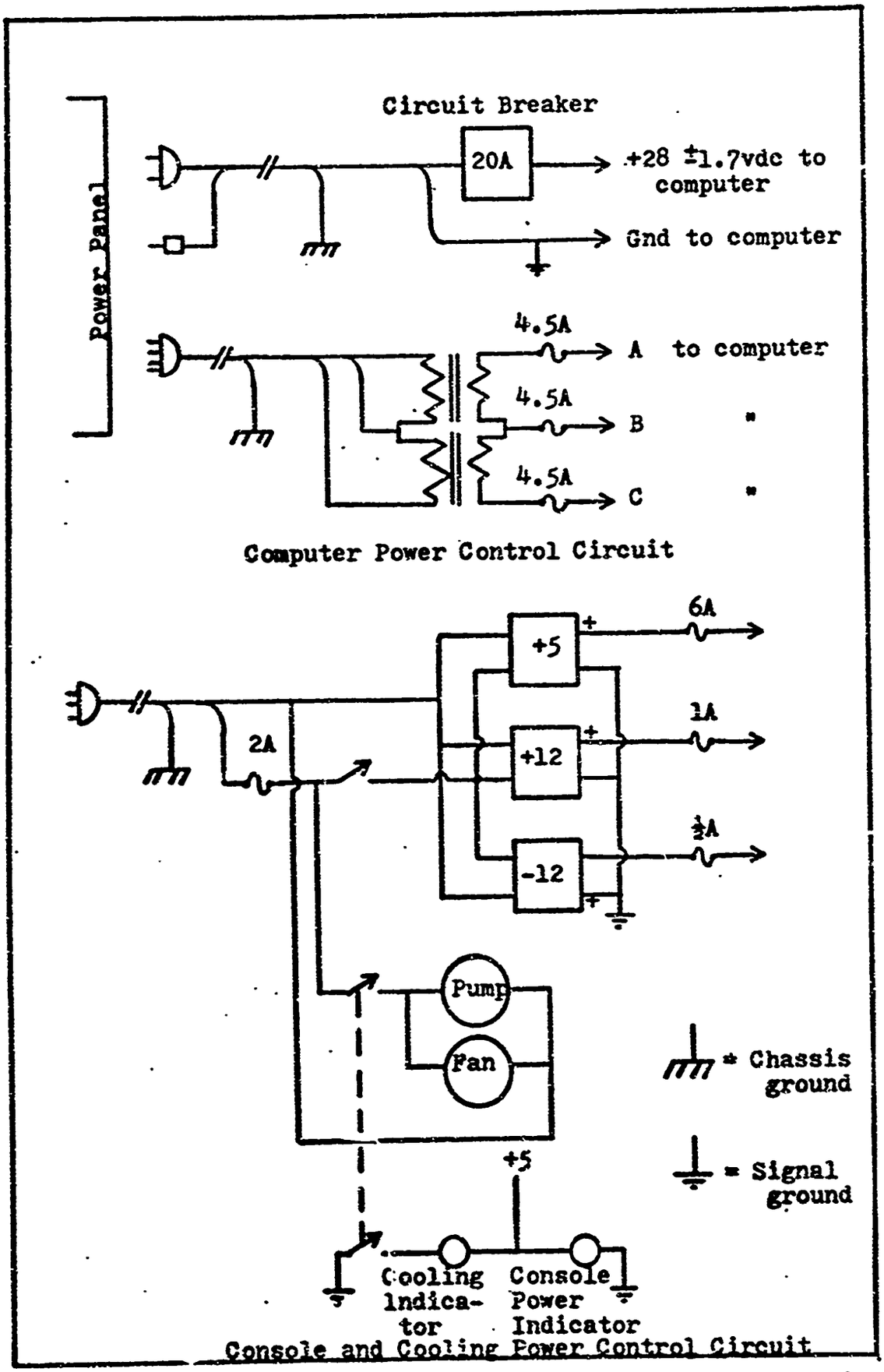


Figure 41. PDU Circuits.

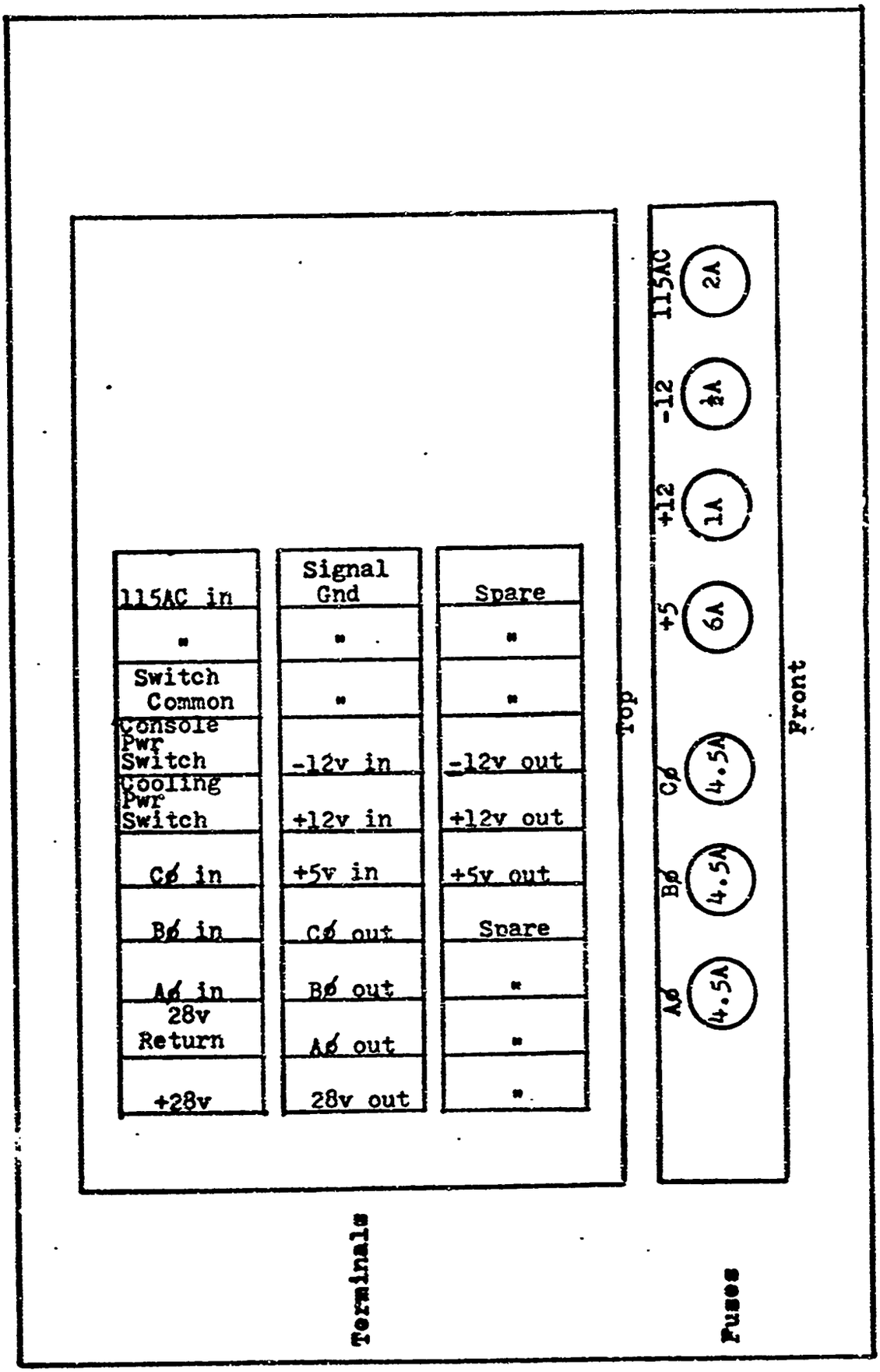


Figure 42. Power Distribution Unit.

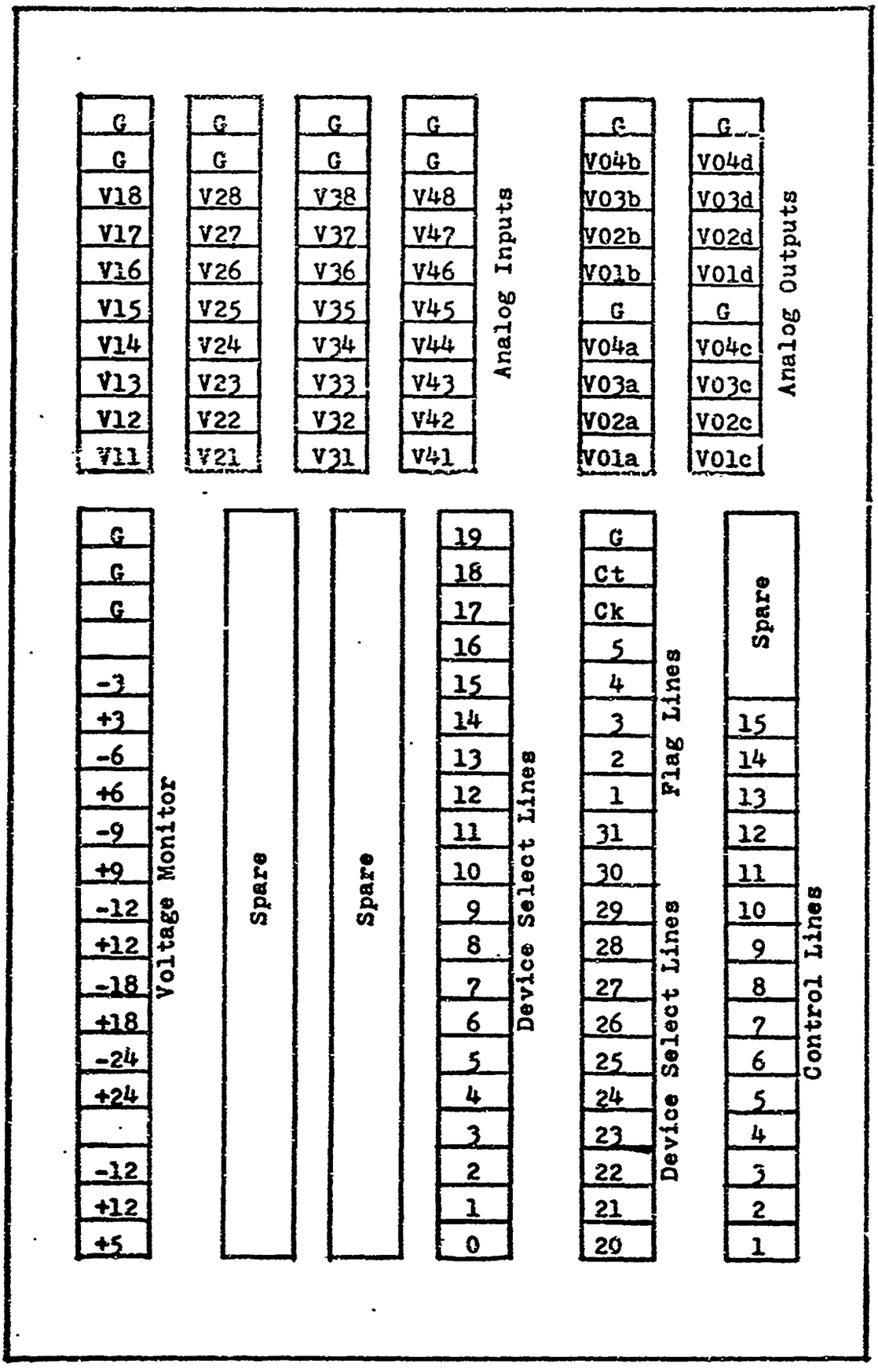


Figure 43. Signal Distribution Unit.

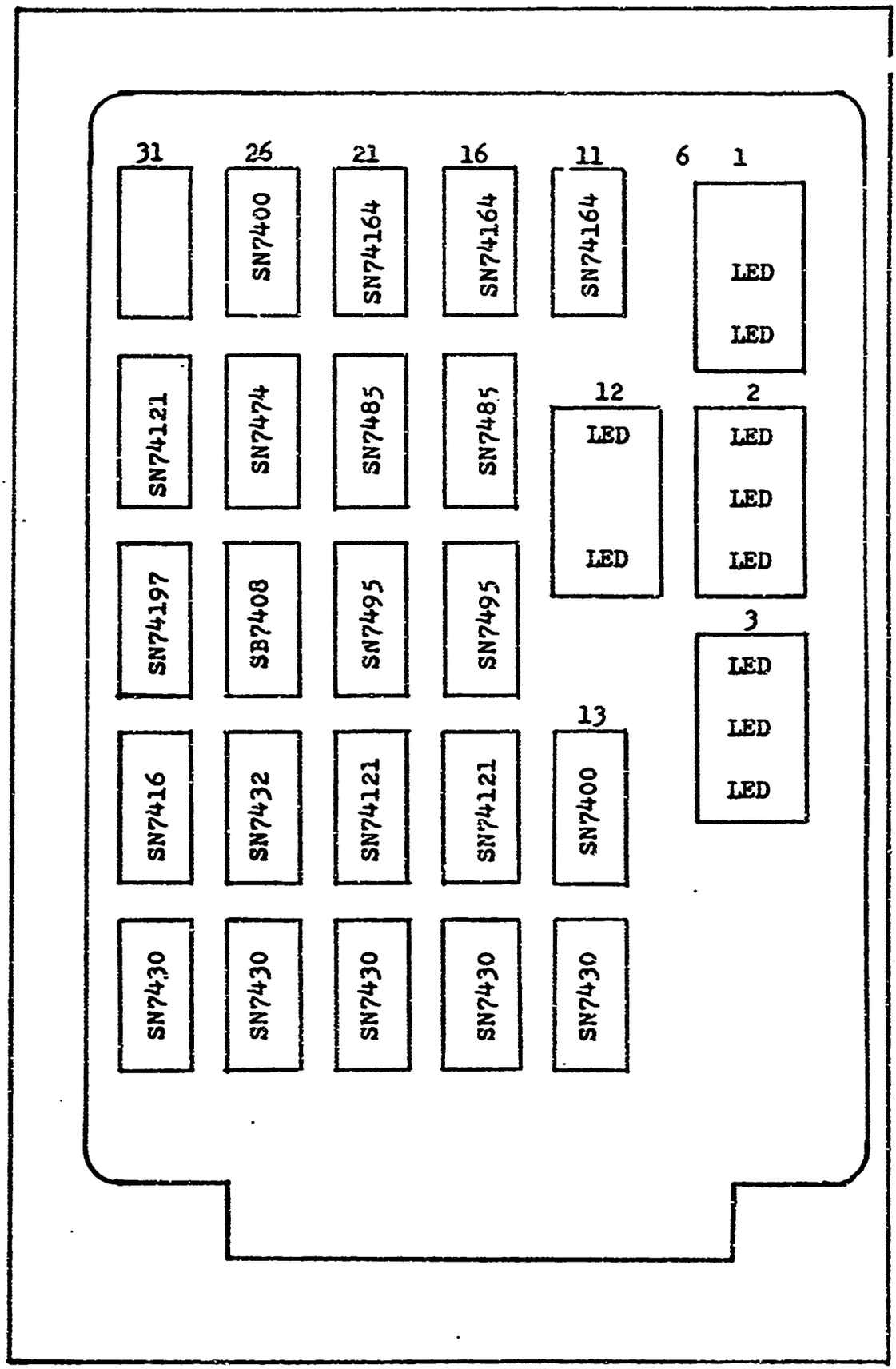


Figure 44. PB Parts Location.

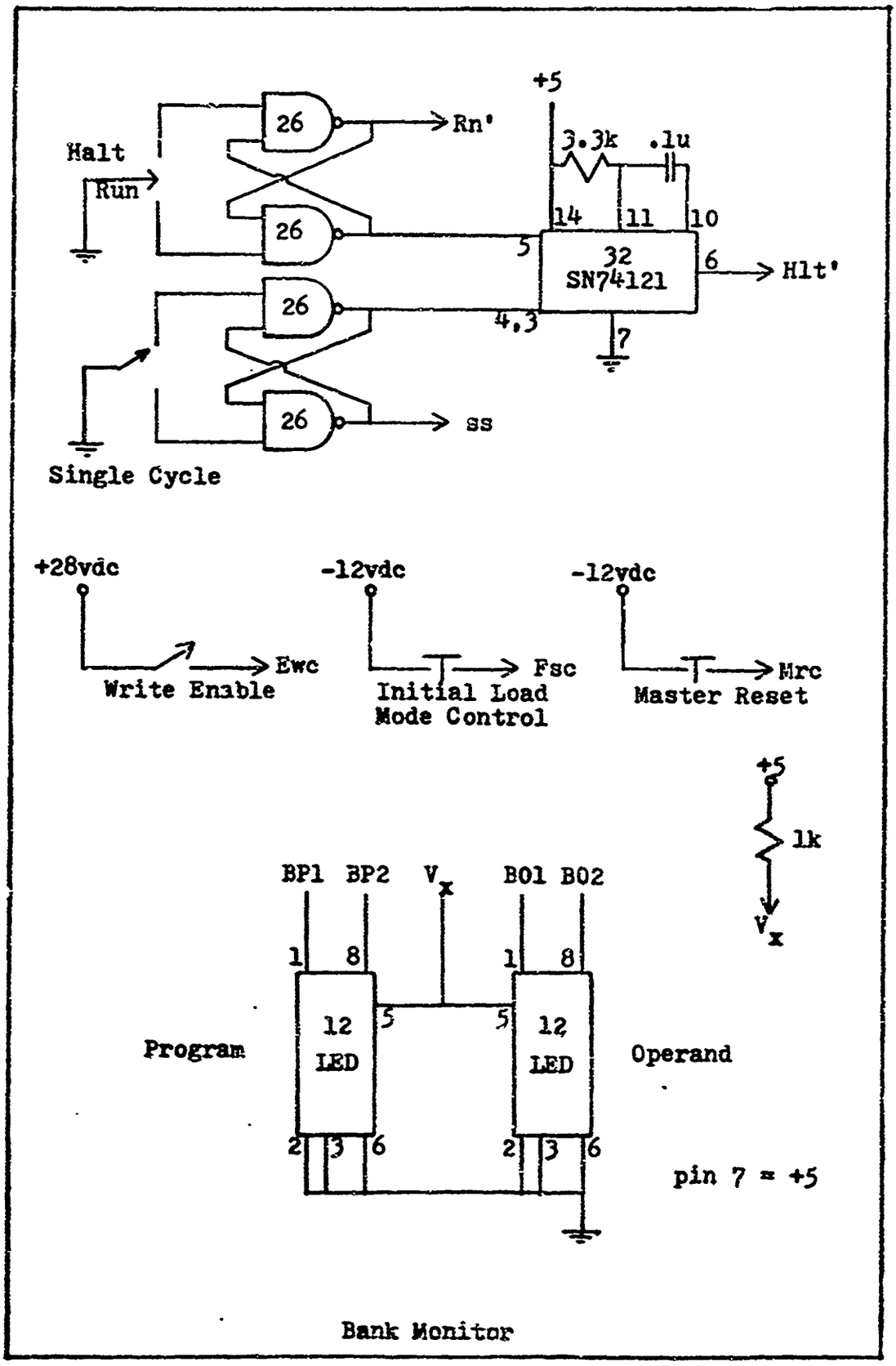


Figure 45. Mode Control and Bank Indicators.

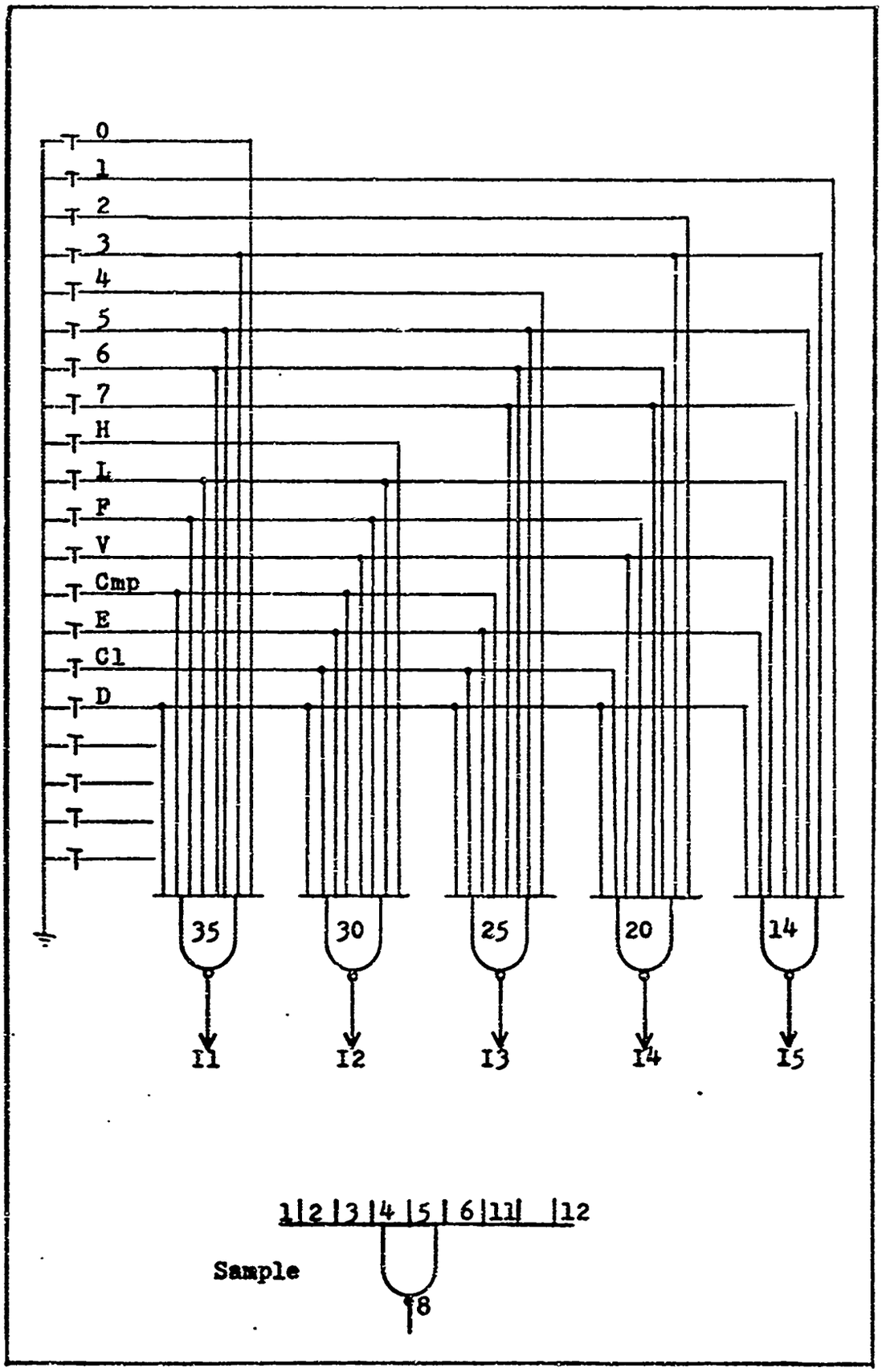


Figure 46. Program Load Schematic (Page 1 of 2).

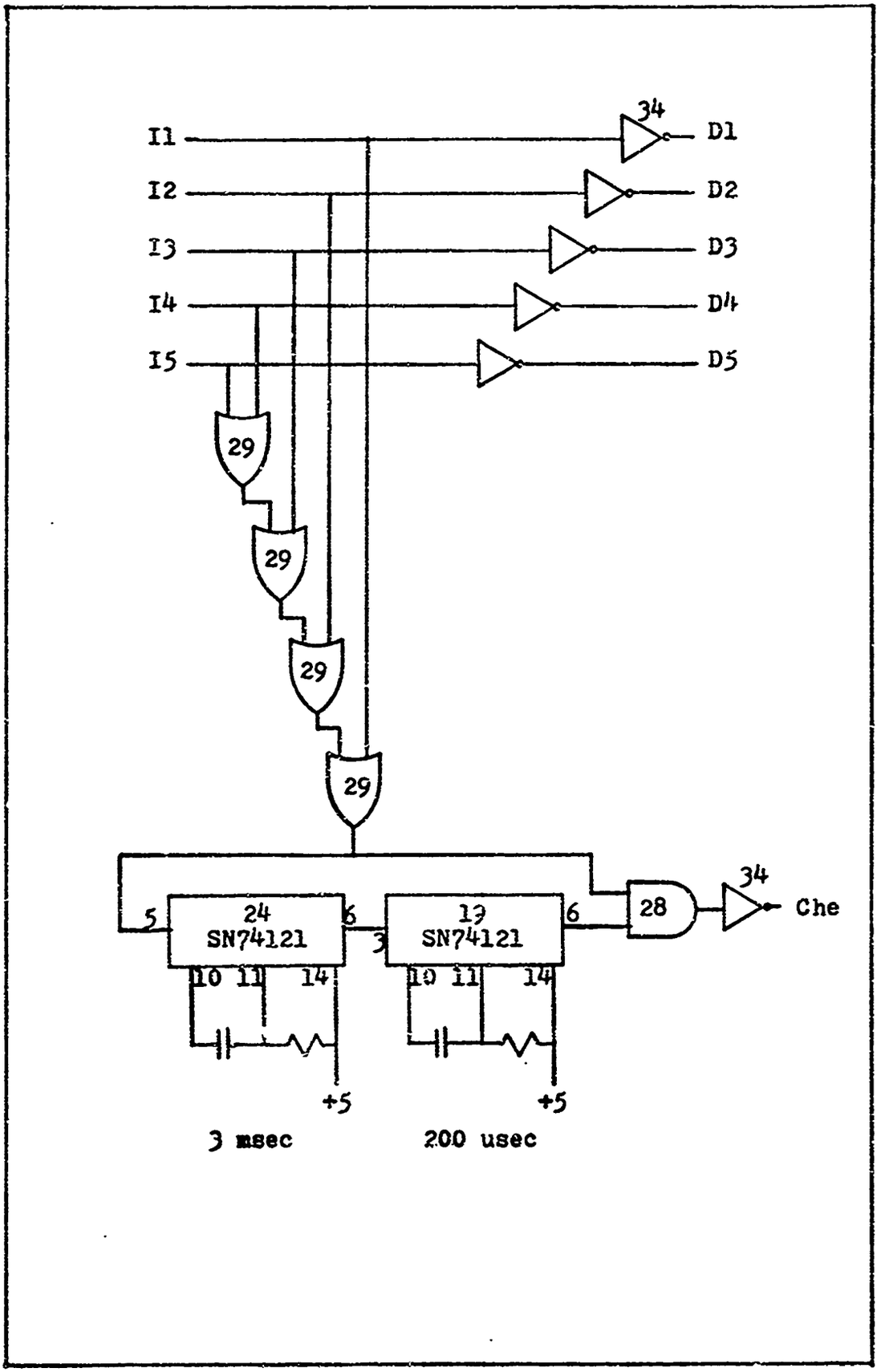


Figure 46. Program Load Schematic (Page 2 of 2).

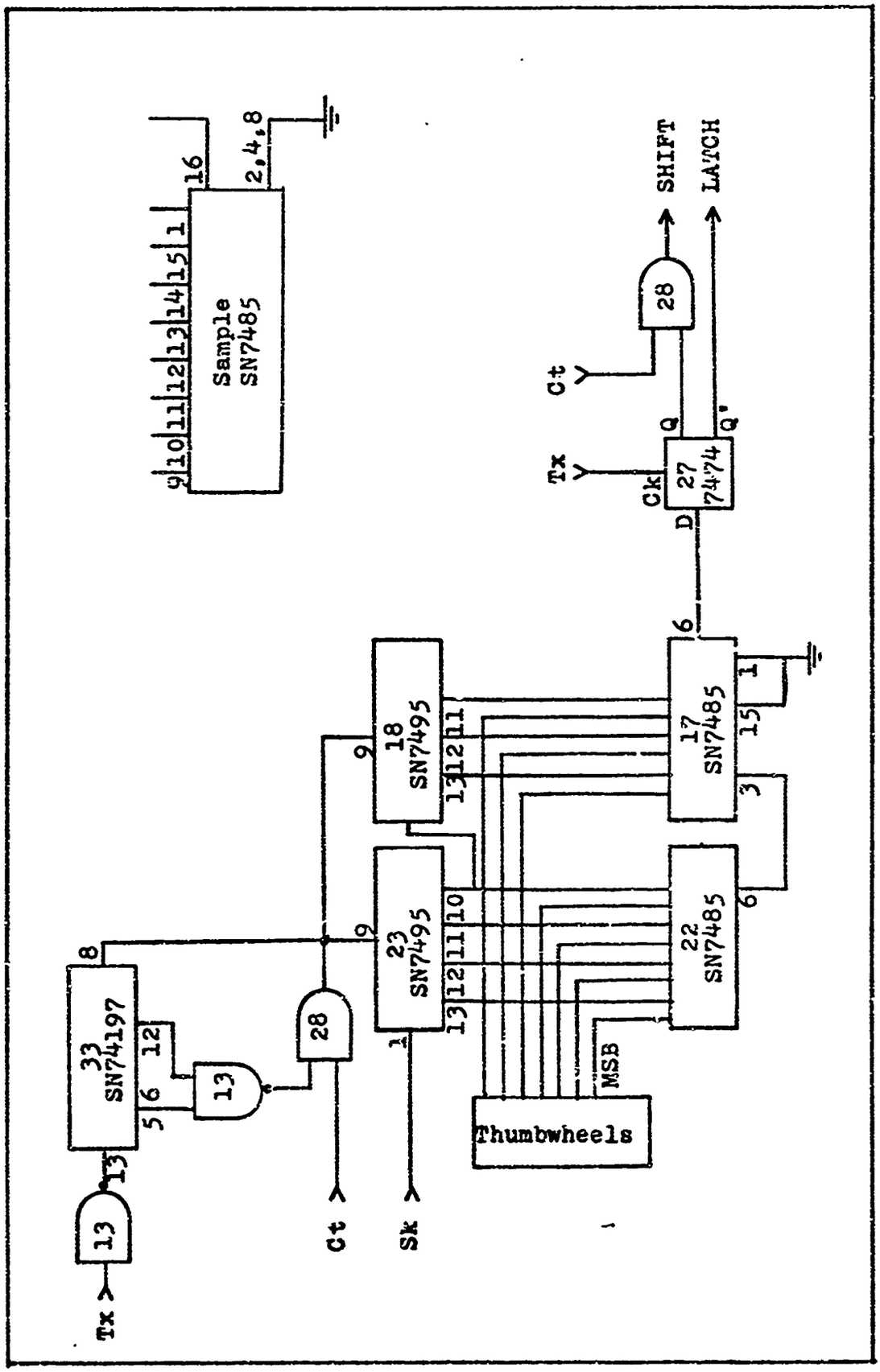


Figure 47. Register Display (Page 1 of 2).

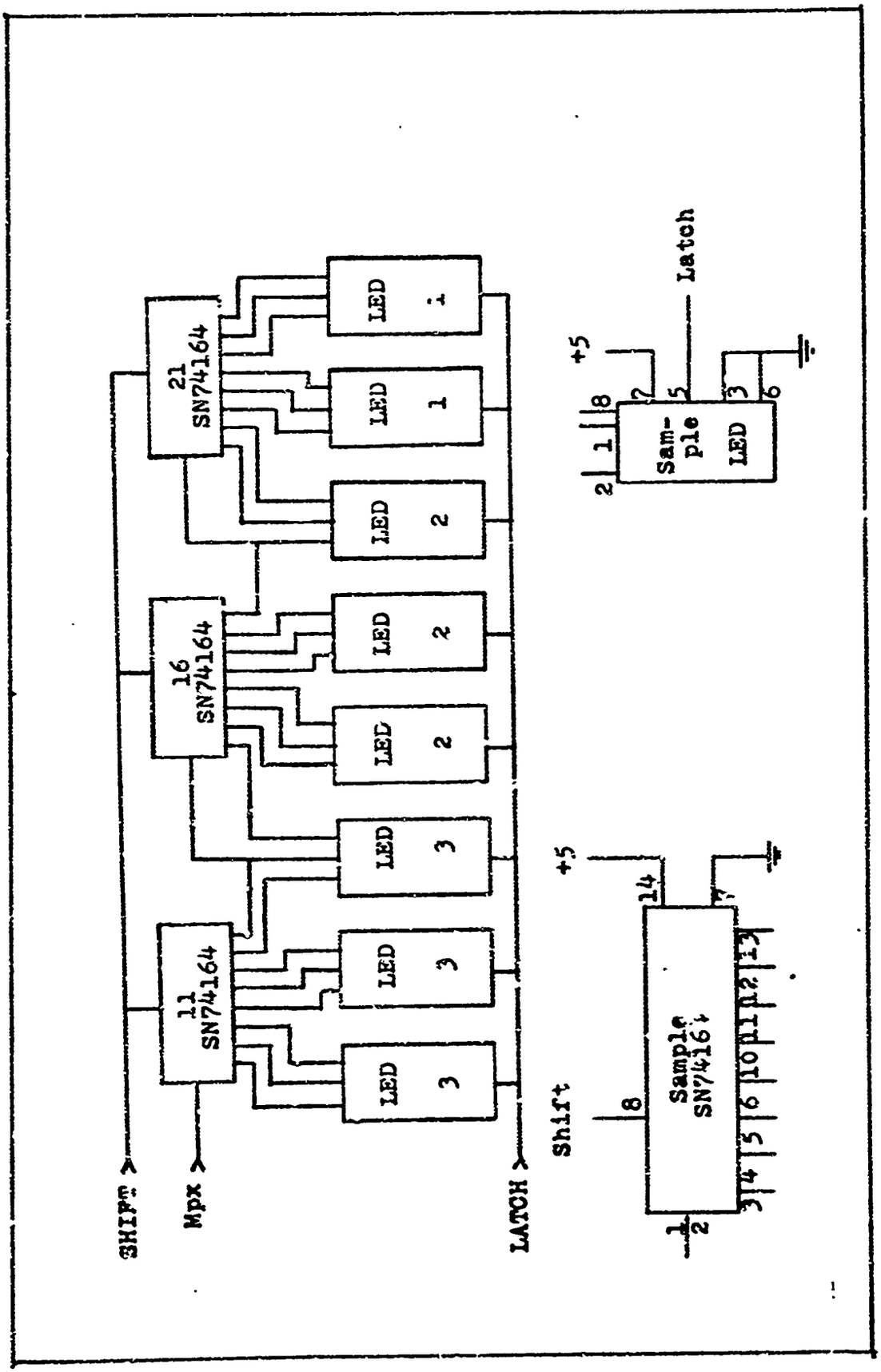


Figure 47. Register Display (Page 2 of 2).

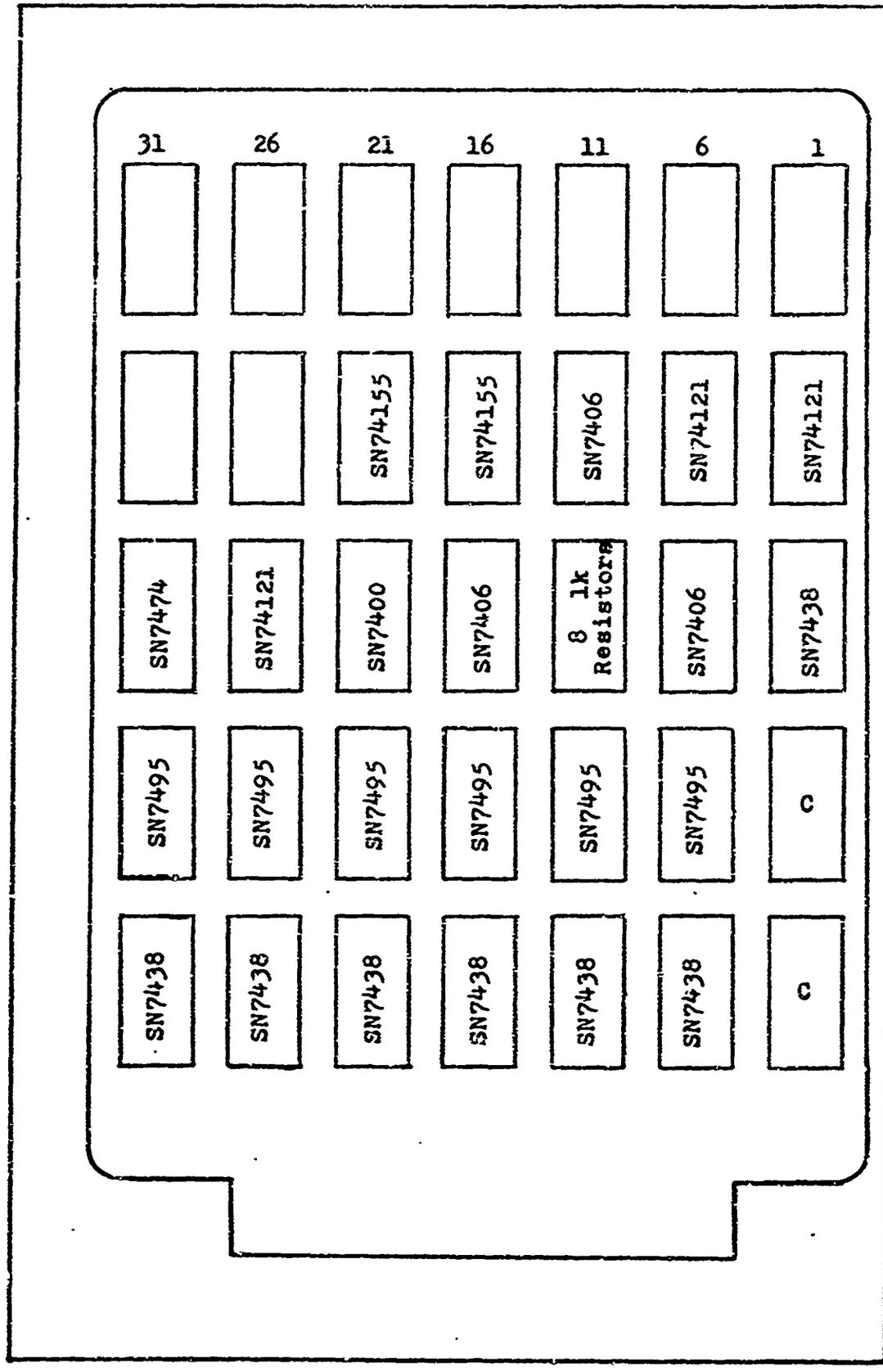


Figure 48. Parts Locations for A.

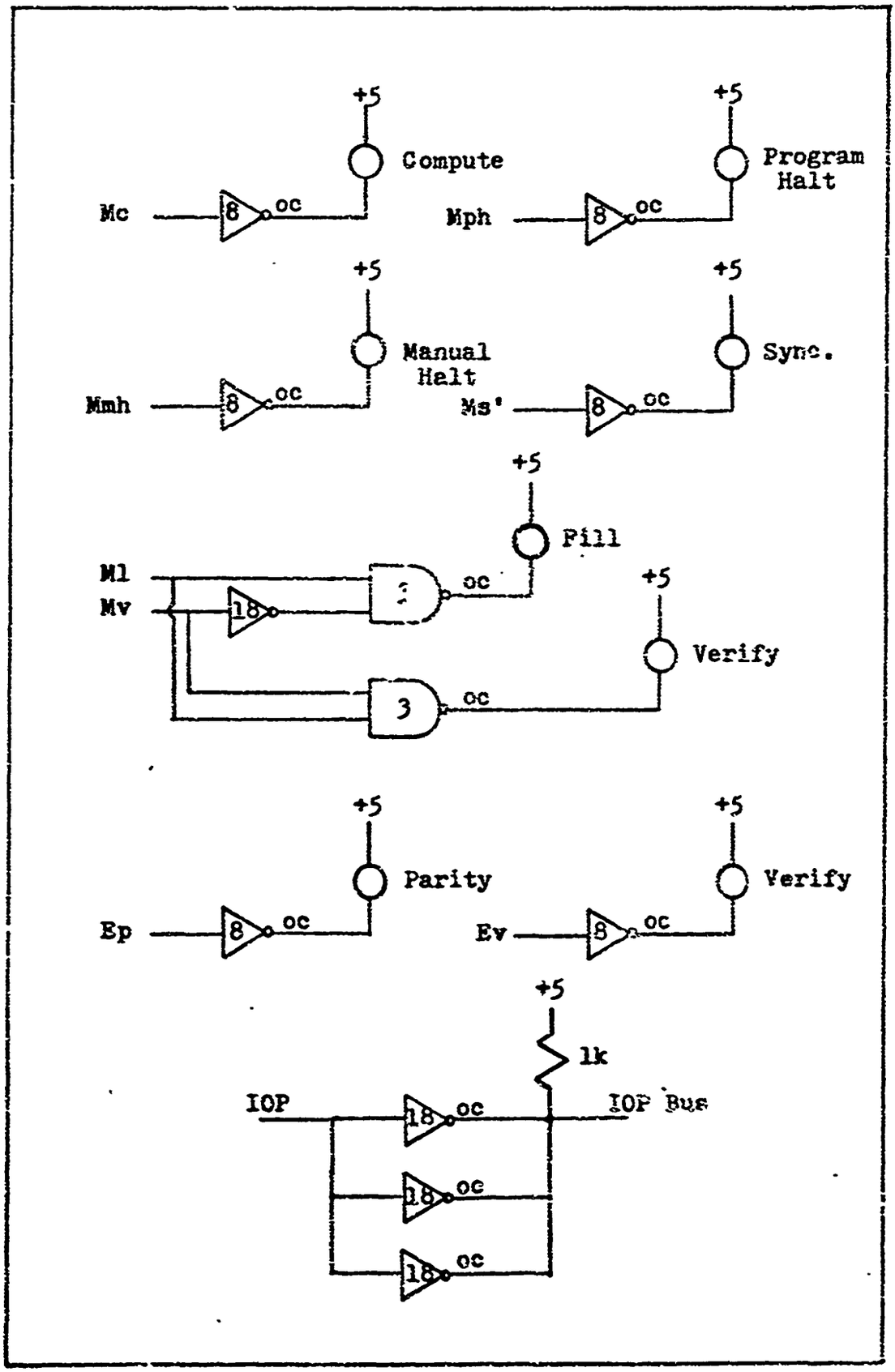


Figure 49. Mode Displays and IOP Driver.

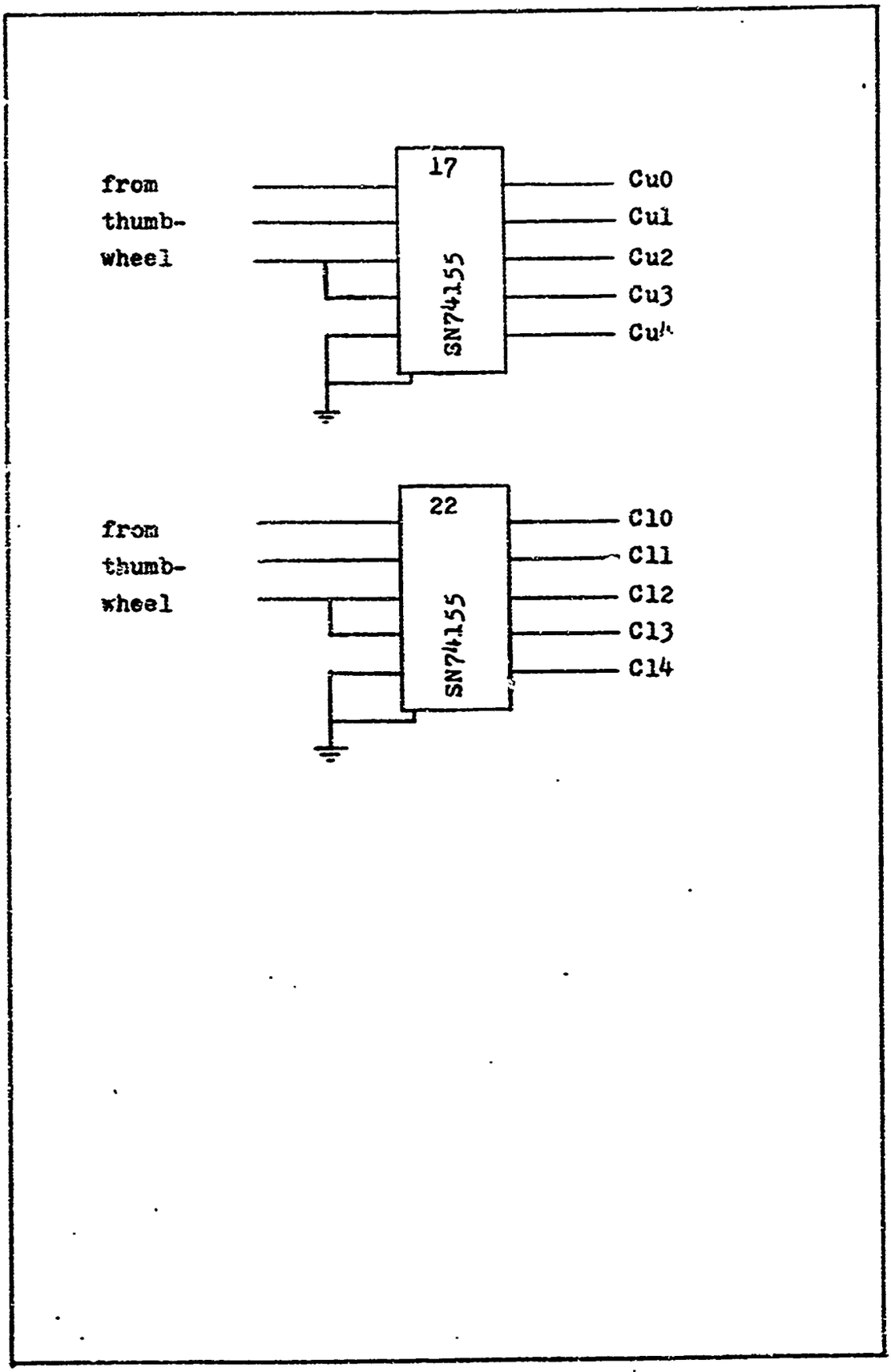


Figure 50. Channel Select.

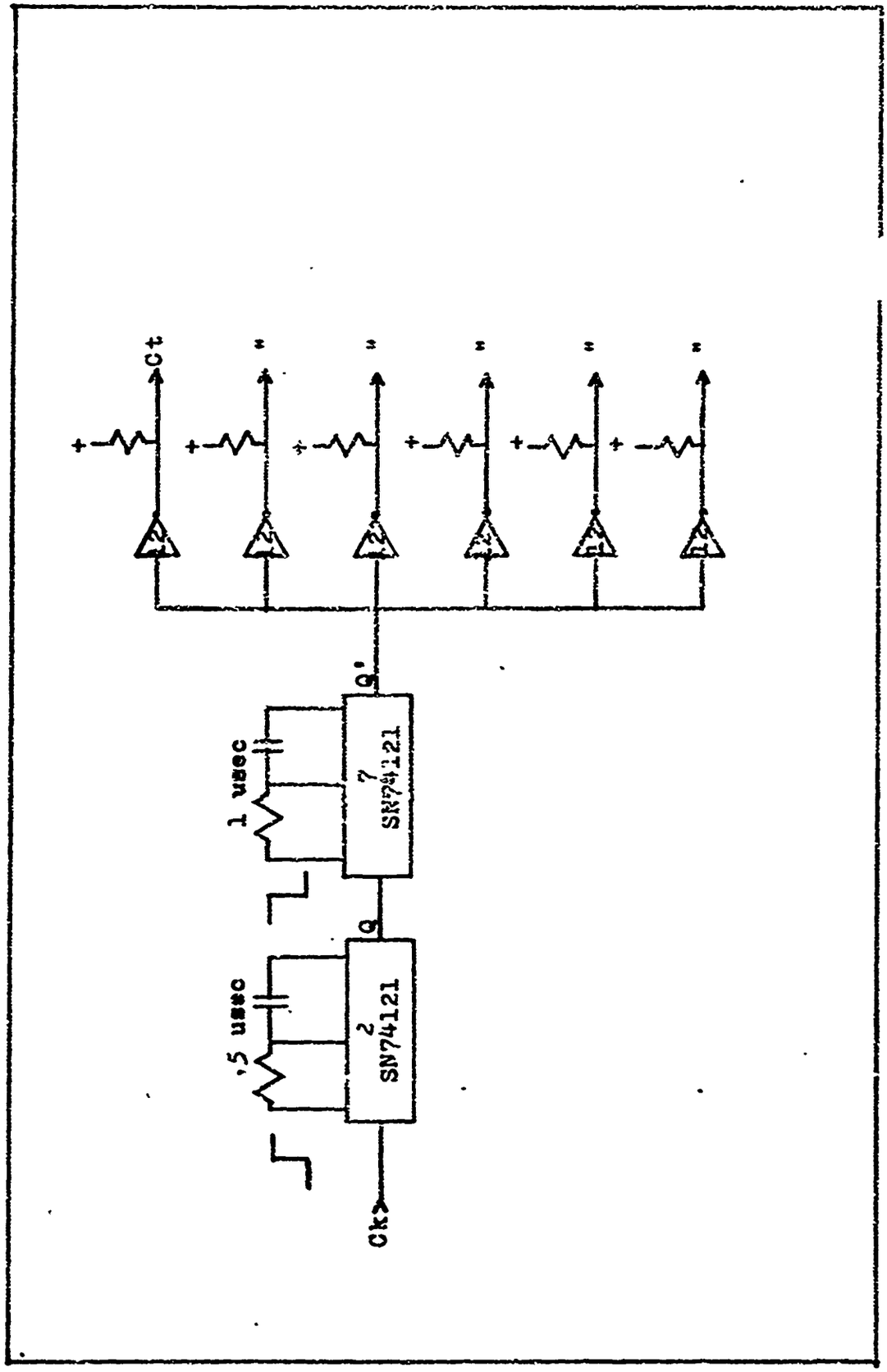


Figure 51. System Clock Schematic.

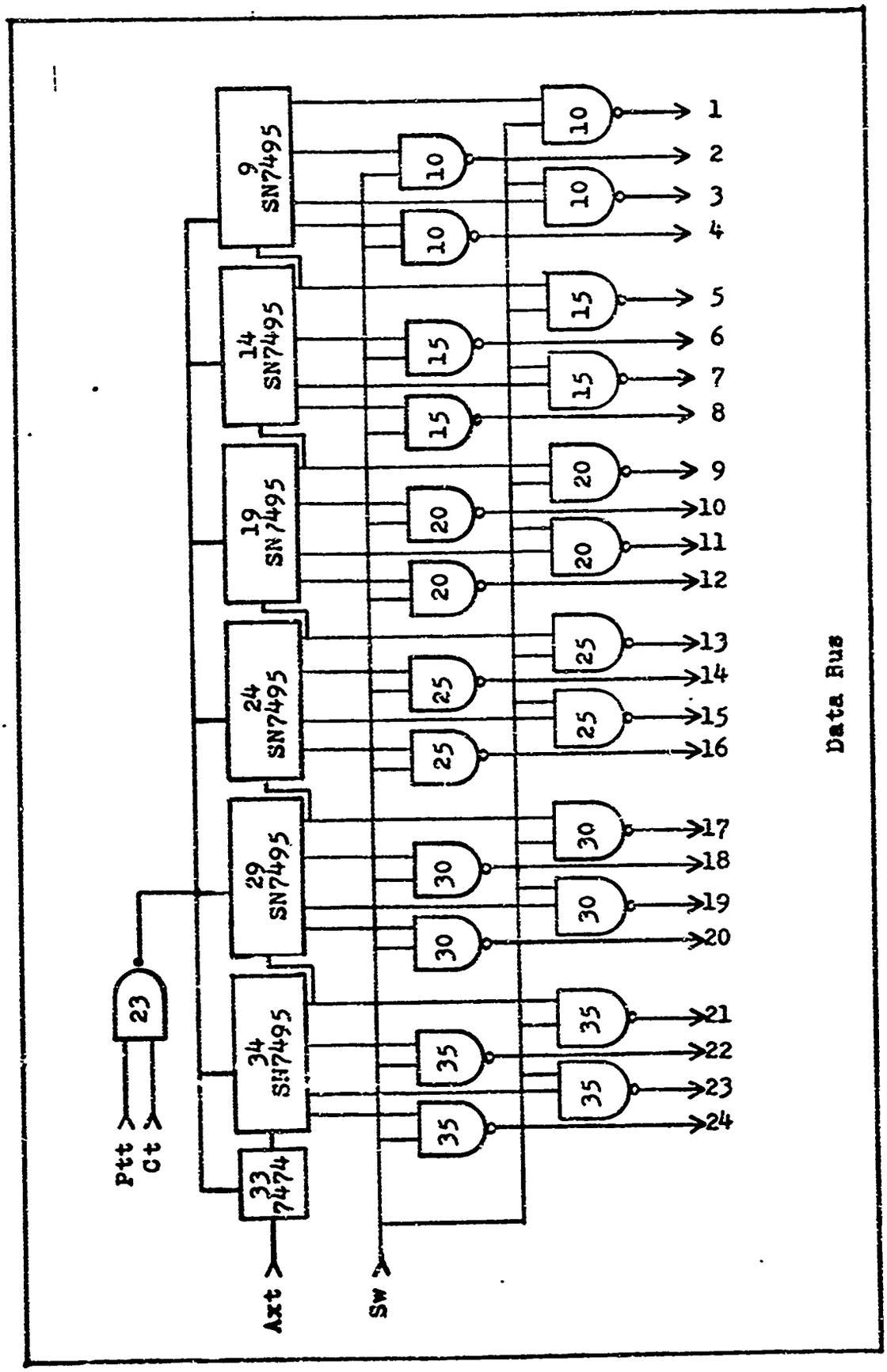


Figure 52. I/O Output Schematic (Page 1 of 2).

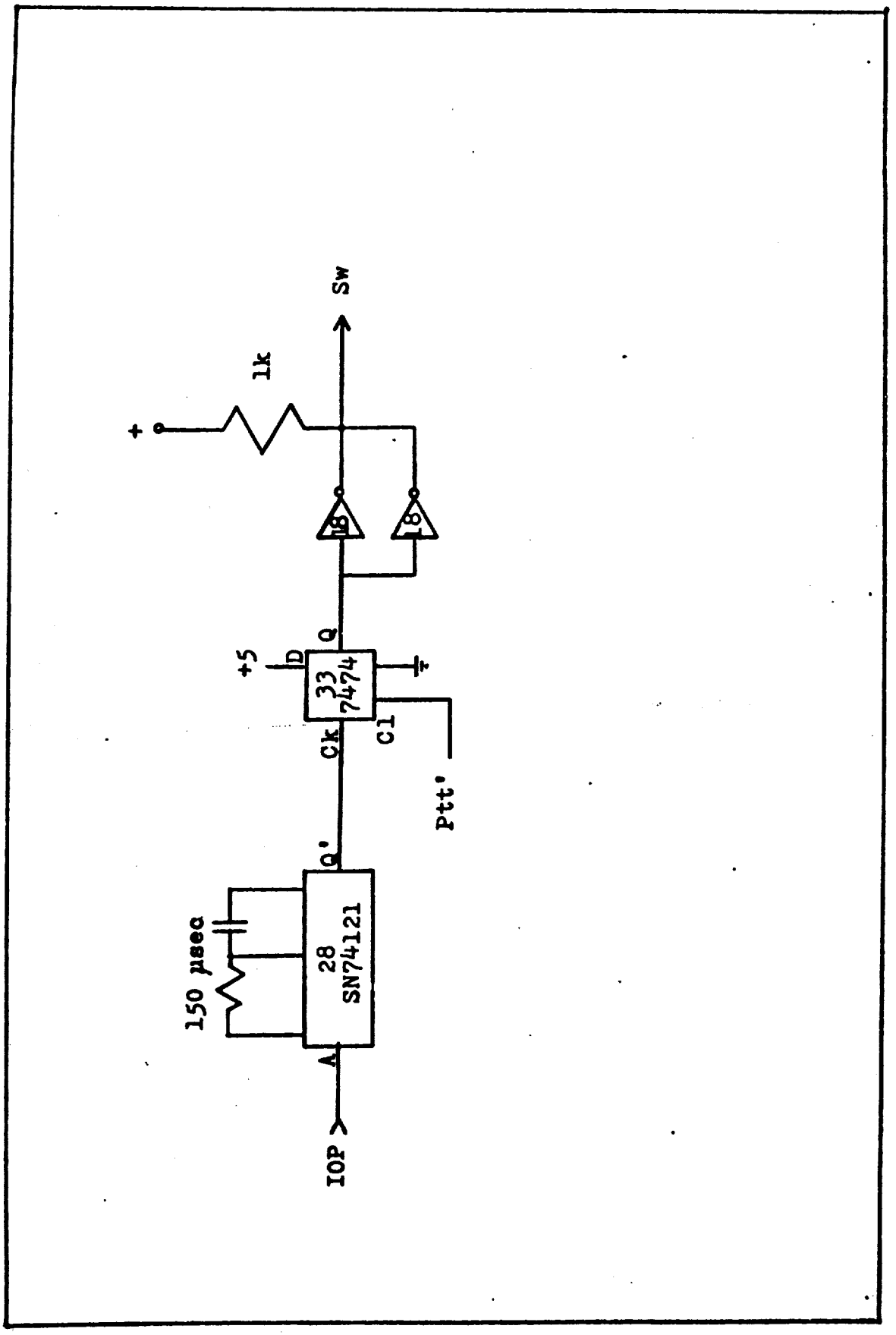


Figure 52. I/O Output Schematic (Page 2 of 2).

Vita

Dennis Craig Reguli was born on 25 October 1950 in Franklin, Indiana. He graduated from high school in Franklin in 1968 and entered the United States Air Force Academy (USAFA). In 1972 he graduated from USAFA, received the degree of Bachelor of Science and a commission in the USAF. He then entered into graduate study at the Air Force Institute of Technology. In December 1972 he married the former Christina Baker of New Whiteland, Indiana.

Permanent address: 161 Brookside Dr.
New Whiteland, Indiana 46184

This thesis was typed by Mrs. Janet M. Lundy.